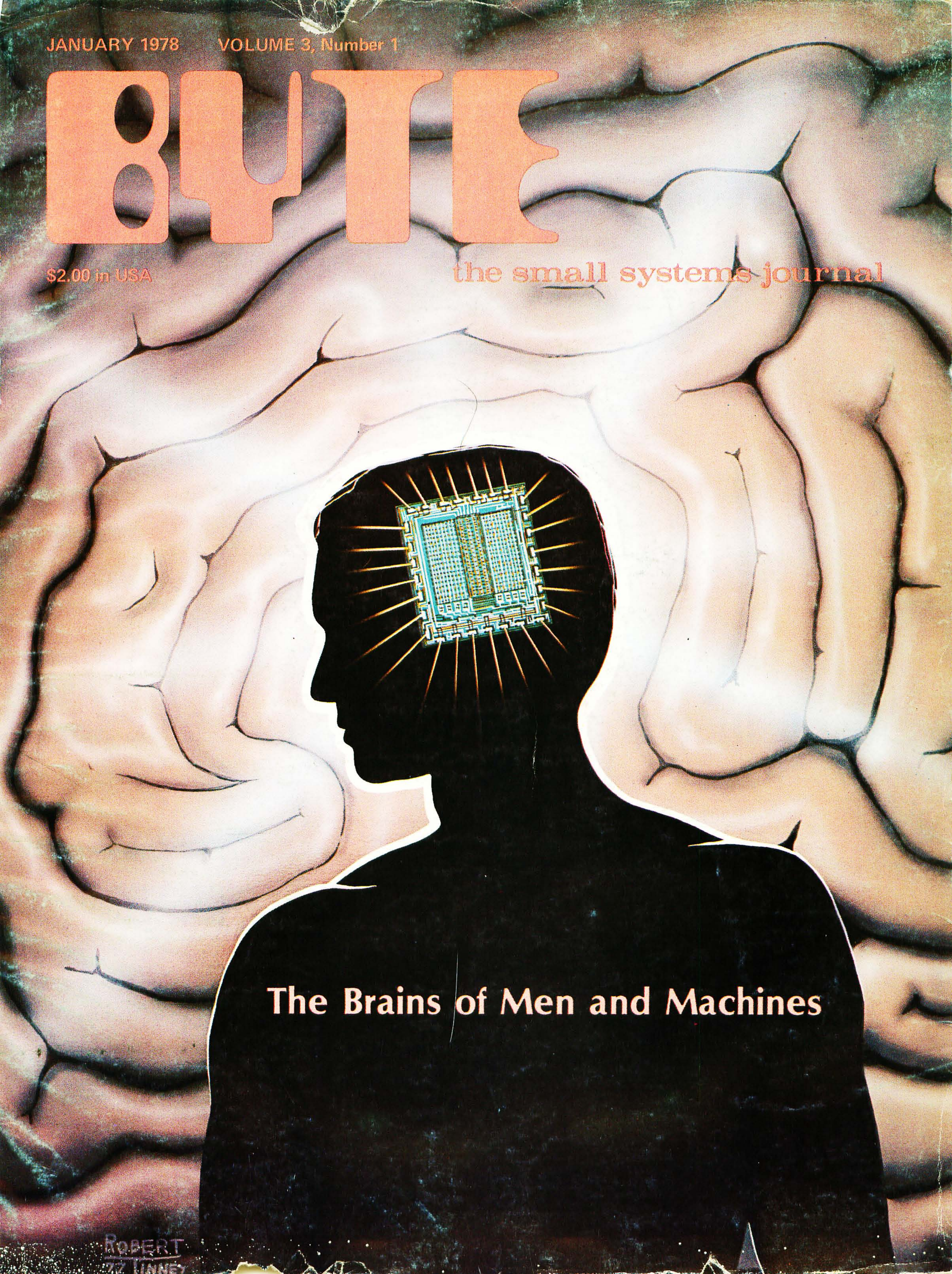

JANUARY 1978 VOLUME 3, Number 1
BYTE
$2.00 in USA
the small systems journal
The Brains of Men and Machines
ROBERT

You can now have the industry's finest microcomputer with that all-important disk drive



The professional-grade microcomputer for professionals

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Loading your programs and files will take you only a few seconds with the new Cromemco Z-2D computer.

You can load fast because the Z-2D comes equipped with a 5″ floppy disk drive and controller. Each diskette will store up to 92 kilobytes.

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CROMEMCO HAS THE SOFTWARE

You can rely on this: Cromemco is committed to supplying quality software support.

For example, here's what's now



ADVANCED CONTROLLER CARD

The new Z-2D is a professional system that gives you professional performance.

In the Z-2D you get our well-known 4-MHz CPU card, the proven Z-2 chassis with 21-slot motherboard and 30-amp power supply that can handle 21 cards and dual floppy drives with ease.

Then there's our new disk controller card with special features:

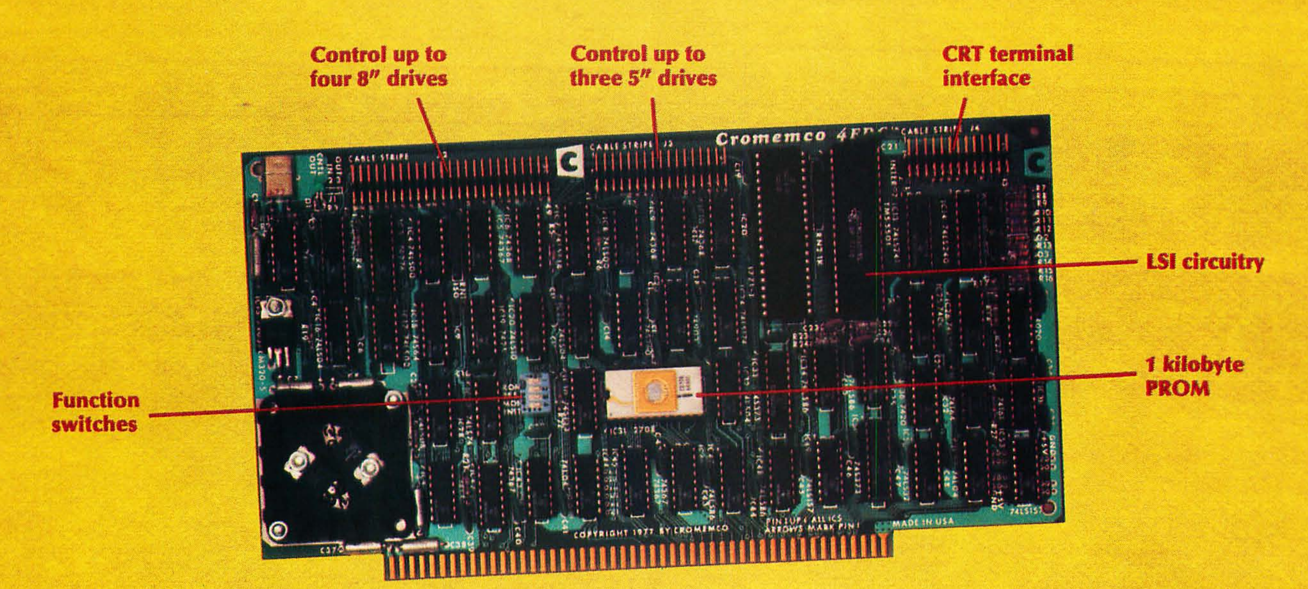
- Capability to handle up to 4

We're able to put all of this including a UART for the CRT interface on just one card because we've taken the forward step of using LSI controller circuitry.

STORE/FACTORY

Contact your computer store or

The easy way to get disk storage, FORTRAN IV, and other programming power



Here's a new disk controller and disk drive combination that will set you up for truly powerful disk storage.

The new controller is extremely versatile. You can use it with **either** our **new 5″ single disk drive** or our **8″ dual disk drive.** In fact, the controller will **interface up to three** 5″ or **four** 8″ drives.

That means you can have enormous disk storage since the new controller puts 92 kilobytes on each side of a 5″ diskette and 256 kilobytes on an 8″ diskette. Recording is in soft-sectored IBM format.

FORTRAN IV AND MORE

You can get still more Cromemco disk operation aids. For example, we also offer FORTRAN IV for our computer users.

And as in so many things, we are the first manufacturer in the field to offer this advanced program for the Z-80 μP.

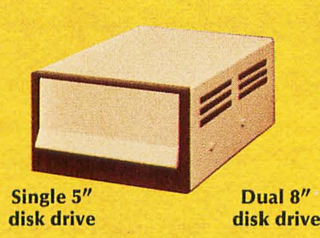
Besides FORTRAN IV we also offer our special BASIC (14-digit precision), our Z-80 Assembler, and now an entertainment diskette with over a dozen of our Dazzler® games.

KEYBOARD CONTROL

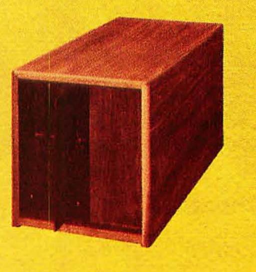
The new Model 4FDC disk controller (supplied in our Z-2D) is for our Z-2 computer or any S-100 bus computer using our Z-80 CPU card.

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Single 5″ disk drive



Dual 8″ disk drive

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This new disk controller equips you for the future as well as for now. Not only can you now have very large storage, but the features of the controller and the standard IBM format protect you from early obsolescence.

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This new card and the disk drives are in production and available.

So contact your computer store or the factory today and you can have the power of FORTRAN IV and a large memory right away.

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Model 4FDC-K Disk Controller kit	$ 395
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Disk drives are complete with power supply, case and cables.

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FORTRAN IV	FDF-S	FDF-L	$95
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In the Queue

BYTE January 1978
Volume 3 Number 1

Foreground

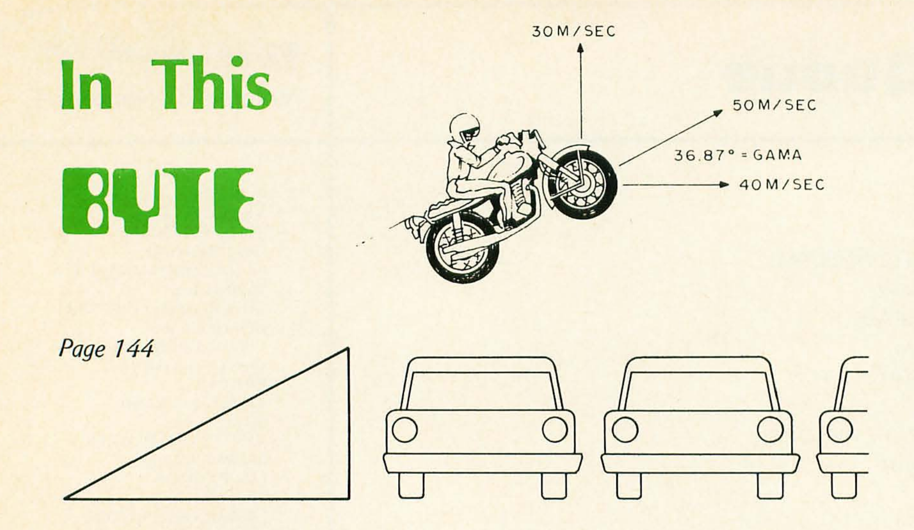
Background

Nucleus



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In This BYTE



Page 144

The compleat robotics experimenter must have a thorough background in biological models of behavior and control, as noted in November's editorial. With this issue, Ernest W Kent begins the first installment of a four part series with **The Brains of Men and Machines, Part 1: Biological Models for Robotics.** Dr Kent has provided readers with a thoroughly understandable introduction to a number of concepts essential to an understanding of the human brain and its simulation in robotic mechanisms. *(Page 11)*

Can the experimenter who runs a small computer business deduct the price of additional memory for the computer? What kind of tax records should the small business keep? If you've been thinking of opening your own small computer business, read Elizabeth M Hughes' **The IRS and the Computer Entrepreneur** for the answers to these and many more tax questions. *(Page 27)*

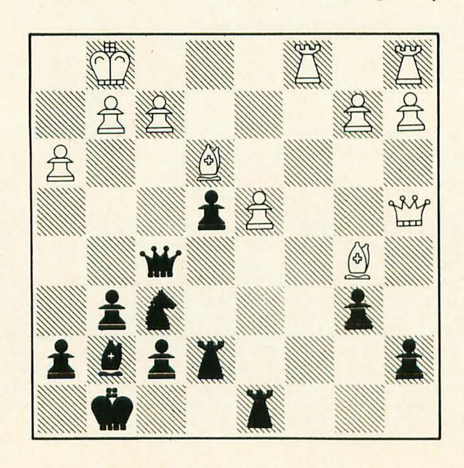
Last month, Steve Ciarcia described an inexpensive 8 channel digital voltmeter driven by a microcomputer. Read **Add More Zing to the Cocktail** in this month's **Ciarcia's Circuit Cellar** and find out how to add multiple ranges, AC and DC input capability and overvoltage protection to the basic circuit. *(Page 37)*

When designing a floppy disk interface, the experimenter is faced with the continuous battle of hardware versus software tradeoffs. David M Allen's **A Floppy Disk Interface** balances the two extremes and shows you how to get a floppy disk system up and running. *(Page 58)*

Paul M Jessop explores the functional organization of **The Motorola 6800 Instruction Set** showing **Two Programming Points of View.** *(Page 84)*

Robert Bumpous provides **A User's Reaction to the SOL-10 Computer** in this issue. Learn a bit more about the Processor Technology computer's design and assembly procedures in Robert's article. *(Page 86)*

In what is probably the world's simplest such design, Walter Banks describes a neat hack, **The Waterloo RF Modulator,** used to convey digitally generated video information from a computer to a standard television set. *(Page 94)*



Page 108

On a battlefield for (intellectual) titans, the forces of black versus white met recently in Toronto. Who won? It was the artificial intelligence experimenters, who demonstrated their nonartificial intelligence in constructing the programs entered in the **Second World Computer Chess Championships,** held last August during the IFIPS show. 16 programs met in logical conflict, with CHESS 4.6 conquering all to win the current title. Turn to Peter Jennings' article for a summary of the action. *(Page 108)*

In **Structured Programming with Warnier-Orr Diagrams, Part 2: Coding the Program,** David A Higgins uses the program design completed in part 1 and demonstrates how to efficiently turn a diagram into a working BASIC program. *(Page 122)*

Continuing the discussion of motion calculated with a personal computer, Stephen Smith's article **Simulation of Motion: Model Rockets and Other Flying Objects** turns to the need for simulating angular degrees of freedom and components of force along different directions. *(Page 144)*

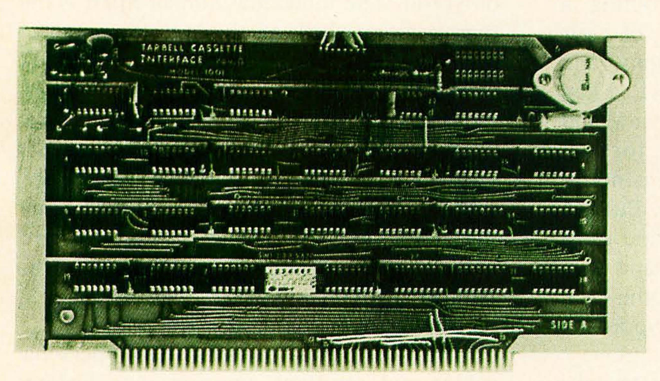
Are you uncertain as to how basic arithmetic operations such as multiplication and division are performed on your computer? If so, Wayne H Ledder's article **A Novice's Eye on Computer Arithmetic** may help you out. *(Page 150)*

Using the RAECO paper tape reader requires a mounting. See Jack Bryant's article on **Mounting a Paper Tape Reader** to see how this unit can be installed in an SwTPC 6800's cabinet. *(Page 161)*

Building a homebrew system based on one of the many microprocessor chips available today is an interesting challenge. In **Notes on Bringing up a Microcomputer,** Sol Libes provides some general background information on the process of wiring and checking out a microcomputer based system. *(Page 162)*

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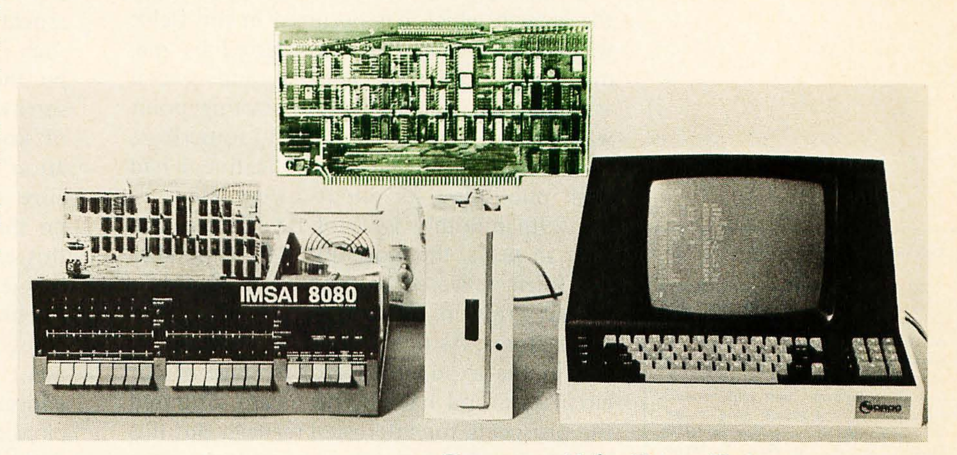


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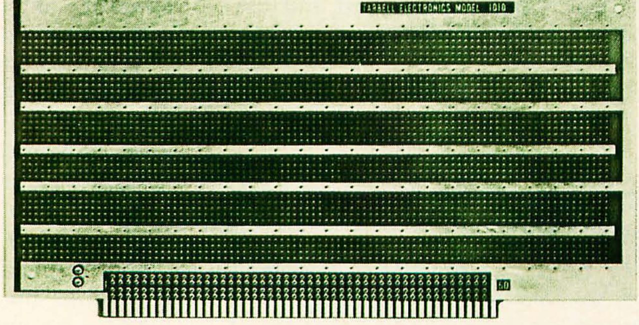
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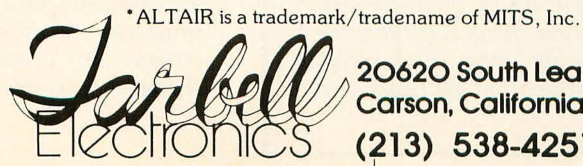


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Editorial

What Is This Phenomenon Personal Computing?

By Carl Helmers

People newly acquainted with the personal computer concept often are baffled by the idea. What does it mean to have and use a personal computer? Why are such computers all of a sudden becoming a prominent technological feature of our culture? In posing these questions and writing a short essay on the subject, a key purpose is to provide a brief overview and summary of personal computing for our newer readers, an exercise which it is necessary to perform from time to time. But the same exercise helps me to review and get a perspective on what is happening, and will, I hope, serve readers familiar with the field as an opportunity for reflection upon the marketplace as it is seen today.

The very fact that I even have to take into account the existence of new readers is a revealing statement about the nature of the growth which has occurred in this field: when BYTE magazine was started by me, my partner Virginia Peschke and several associates in mid-1975, the starting point was essentially zero—the 250-odd subscribers to a newsletter technical publication I had been publishing for about a year. Now, as the 29th monthly issue of BYTE magazine goes to press, the November 1977 issue has just been delivered to over 105,000 people by subscription or sales in over 600 computer stores. As nearly as we can tell, we are still in the exponential growth stage of our circulation and have by no means saturated the prospects for interested readers. But this is only a reflection upon the industry as a whole. We could not support such a large circulation if it weren't for the fact that there is a large and active group of manufacturers who are producing and selling the products which our readers need and use as personal computing oriented people. Why?

Ours is a culture of the mind. Western civilization's most prominent characteristic is that it salutes the individual thinking being (and indeed its generalizations to any sentient beings which may exist in the universe). The individual human mind is the temple from which all the appurtenances of modern civilization spring. Our market oriented civilization, more than any other, tends to recognize and promote the products of the individual thinker, whether engineer, novelist, scientist, manager, student, capitalist, lawyer or a host of other specializations. To think is the standard human mode of operation, a part of the built-in equipment which has evolved in the species Homo sapiens.

The fact that humans have personal values and resultant emotions and feelings is in no way inconsistent with this description of humanity. If I know joy at some aspect of living, the fact that I can perceive such is often enhanced, if not made possible, by the operation of my mind. If I know sorrow at some other aspect of living, the act of knowing is made possible by the operation of my mind. And of course, I generalize this: I am not the only active being on this planet. Every one of the readers of this essay is a unique variation on a similar theme. Into this milieu of a culture which celebrates and promotes individual achievement as a way of life springs an achievement of numerous individuals working in concert, the modern large scale integrated circuit, the computer on a chip. The result is today's real life version of what might have been a science fiction scenario in past decades.

The human mind from which this achievement springs is a portable, fairly efficient, and quite remarkable thinking machine, a product of countless millennia of evolution where the guiding standard has been success as an organism in a complicated environment. The human mind is intricately involved with the phenomenon which is the computer as we know it in this culture: the computer is a genuine manifestation of a hard to define science fiction concept, the "thought amplifier." As a practical reality, it involves no technological extensions of biology, no mystical force fields, not one iota of built-in enmity for humans. The computer in all its uses is nothing more than an extension of the mind of its user. The programs which we all put into our computers are crystallizations of our own thought processes in a form which can be

Continued on page 142

Articles Policy

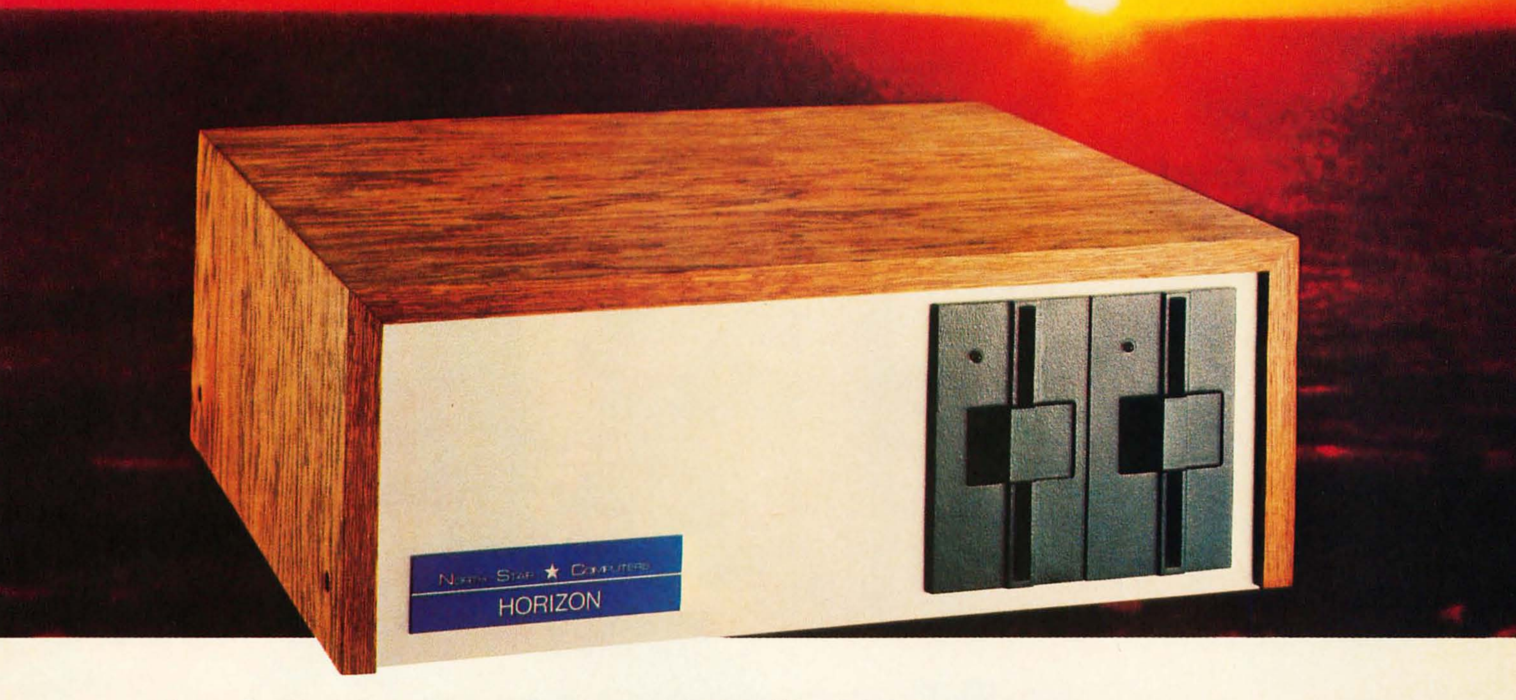
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Articles which are accepted are purchased with a rate of up to $50 per magazine page, based on technical quality and suitability for BYTE's readership. Each month, the authors of the two leading articles in the reader poll (BYTE's Ongoing Monitor Box or "BOMB") are presented with bonus checks of $100 and $50. Unsolicited materials should be accompanied by full name and address, as well as return postage. ■

So What Is the Current Personal Computer User Like?

Scheduled for mailing January 15 1978 is a new BYTE reader survey. Approximately 5000 readers selected at random from our subscription mailing list in December will receive a detailed questionnaire concerning numerous aspects of personal computer use and enjoyment, as well as normal demographic data. A summary of the statistics from this survery will be published in BYTE after the analysis is completed (as was done last year). If your name is picked, we'd appreciate your response to the survey, in the interest of creating an accurate statistical record of what is happening and has happened in this field.

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Look To The North Star HORIZON Computer.

HORIZON™— a complete, high-performance microprocessor system with integrated floppy disk memory. HORIZON is attractive, professionally engineered, and ideal for business, educational and personal applications.

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The Z80A processor operates at 4MHZ — double the power of the 8080. And our 16K RAM board lets the Z80A *execute at full speed*. HORIZON can load or save a 10K byte disk program in less than 2 seconds. Each diskette can store 90K bytes.

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HORIZON-1 $1599 kit; $1899 assembled.
HORIZON-2 $1999 kit; $2349 assembled.

16K RAM—$399 kit; $459 assembled; Parity option $39 kit; $59 assembled. FPB $259 kit; $359 assembled. Z80 board $199 kit; $259 assembled. Prices subject to change. HORIZON offered in choice of wood or blue metal cover at no extra charge.

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Only Apple II makes it that easy. It's a complete, ready to use computer, not a kit. At $1298, it includes video graphics in 15 colors. It includes 8K bytes ROM and 4K bytes RAM—easily expandable to 48K bytes using 16K RAMs (see box). But you don't even need to know a RAM from a ROM to use and enjoy Apple II. For example, it's the first personal computer with a fast version of BASIC permanently stored in ROM. That means you can begin writing your own programs the first evening, even if you've had no previous computer experience.

The familiar typewriter-style keyboard makes it easy to enter your instructions. And your programs can be stored on—and retrieved from—audio cassettes, using the built-in cassette interface, so you can swap with other Apple II users.

You can create dazzling color displays using the unique color graphics commands in Apple BASIC. Write simple programs to display beautiful kaleidoscopic designs. Or invent your own games. Games like PONG—using the game paddles supplied. You can even add the dimension of sound through Apple II's built-in speaker.

But Apple II is more than an advanced, infinitely flexible game machine. Use it to teach your children arithmetic, or spelling for instance. Apple II makes learning fun. Apple II can also manage household finances, chart the stock market or index recipes, record collections, even control your home environment.

Right now, we're finalizing a peripheral board that will slide into one of the eight available motherboard slots and enable you to compose music electronically. And there will be other peripherals announced soon to allow your Apple II to talk with another Apple II, or to interface to a printer or teletype.



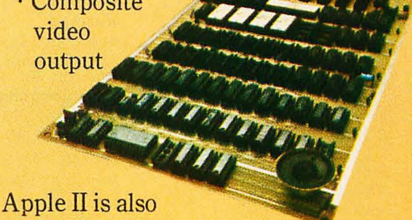
Apple II is designed to grow with you as your skill and experience with computers grows. It is the state of the art in personal computing today, and compatible upgrades and peripherals will keep Apple II in the forefront for years to come.

Write us today for our detailed brochure and order form. Or call us for the name and address of the Apple II dealer nearest you. (408) 996-1010. Apple Computer Inc., 20863 Stevens Creek Boulevard, Bldg. B3-C, Cupertino, California 95014.

Apple II™ is a completely self-contained computer system with BASIC in ROM, color graphics, ASCII keyboard, lightweight, efficient switching power supply and molded case. It is supplied with BASIC in ROM, up to 48K bytes of RAM, and with cassette tape, video and game I/O interfaces built-in. Also included are two game paddles and a demonstration cassette.

SPECIFICATIONS

- **Microprocessor:** 6502 (1 MHz).
- **Video Display:** Memory mapped, 5 modes—all Software-selectable:
  - Text—40 characters/line, 24 lines upper case.
  - Color graphics—40h x 48v, 15 colors
  - High-resolution graphics—280h x 192v; black, white, violet, green (12K RAM minimum required)
  - Both graphics modes can be selected to include 4 lines of text at the bottom of the display area.
  - Completely transparent memory access. All color generation done digitally.
- **Memory:** up to 48K bytes on-board RAM (4K supplied)
  - Uses either 4K or new 16K dynamic memory chips
  - Up to 12K ROM (8K supplied)
- **Software**
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  - 8-slot motherboard
  - Apple game I/O connector
  - ASCII keyboard port
  - Speaker
  - Composite video output



Apple II is also available in board-only form for the do-it-yourself hobbyist. Has all of the features of the Apple II system, but does not include case, keyboard, power supply or game paddles.

PONG is a trademark of Atari Inc.

*Apple II plugs into any standard TV using an inexpensive modulator (not supplied).



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The Brains of Men and Machines

Part 1: Biological Models for Robotics

Ernest W Kent, Associate Professor
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The idea of a machine that thinks like a man has always fascinated us. If we talk about substantial improvements in processor design, it is relegated to a few technical journals, but if we talk about robots, or write stories about computers with personalities, or make movies about HAL, everyone gets interested, and computer buffs stay up all night trying to figure out how to make their machines behave like that. An artificial "intelligence," in the sense in which we apply that term to our own thought processes, has been a recurring theme dating back to antiquity, despite the fact that no such machine has ever existed. I don't know why this is so, perhaps it springs from a desire to understand our own thoughts, or perhaps the human race is just lonely. We keep hoping for dolphins and Martians to start talking to us too. Whatever the reason, the idea is a potent one, and an enduring source of interest.

Why then don't we build computers that think like men? Well, people have certainly tried, and some very elegant software has been created towards that end, but the results have always been frustratingly limited. You have all heard the old adage that a computer to equal the human brain would require a machine the size of the Empire State Building with the electrical output of Niagara Falls to power it, but that was always just an excuse. Aside from the fact that whoever coined that notion didn't have any idea of what a brain-like computer would require, the fact is that we would have built it anyway, if we'd known how. Moreover, when that guess was made, we were making computers out of 12AX7s, and it's a long way from the 12AX7 to the Z-80. We would certainly build that machine today, if we knew how. What then is the problem? Our big fast machines can do elegant and complex mathematics, even proofs, far beyond our own powers, yet we have the greatest difficulty making them display even the slightest degree of common sense. The System 370 can do amazing things with numbers, but it wouldn't have the intelligence to duck if you swung a club at it. A frog could do better at dealing with its environment.

I assure you that the problem has nothing to do with any mysterious properties of the brain. If we have learned anything about the brain, it is that it is a machine. A complex machine to be sure, but a machine nonetheless. This notion frequently upsets people; they are bothered by the suggestion that they might be "only a machine." I think that this is the wrong interpretation. The statement that the brain is a machine does not mean that it is "only" a machine in the sense of the simple machines of limited ability that we have produced. Rather, it is a statement that extends our concept of what a machine can do. It does not denigrate what the brain can do. Of course, it raises the possibility that we *can* design a machine that thinks like a man, with all of the attendant problems of philosophy and theology that that raises.

One could take refuge in the notion that brain and mind may somehow be different, but the evidence is that when the brain is manipulated experimentally, all of our mental processes, our sensations and perceptions, our feelings and emotions, our intellectual processes, our memories, even our states of consciousness are manipulated too. The evidence suggests that this manipulation

is predictable and occurs in the same fashion in all individuals.

Why are we having so much trouble making our computers behave in brain-like fashions if both are machines and both information processing machines at that? I think the answer is that we are trying to make a wrench do a screwdriver's job. What I mean is that while all information processing machines may theoretically be capable of imitating all others, Turing didn't say that all had to be built to handle all problems with equal ease. In point of fact, the brain's architecture is quite different from that of computers as we customarily build them, and different in ways that are very instructive with regard to the problem of building a "thinking machine."

The brain and the computer have both developed in an evolutionary manner, with "survival of the fittest" determining what features were retained and what were discarded. The differences in their designs arise from the fact that nature and computer engineers have different notions of what constitutes "fittest." There are two aspects to this difference: the nature of the problems the machine is required to solve, and the nature of the hardware available to build the machine. The successful brains, the ones whose genes contributed to the next generation, were the ones that had good designs for solving problems like recognizing and avoiding dinosaurs, and recognizing and catching frogs. Ability at higher mathematics was never a very important criterion in determining successful brain design, and our poor brains get quickly strained when they're required to do much of it. Computer design was judged from the beginning in terms of its success at mathematical function, and as a result they are very good at it, but very bad at catching frogs.

The kind of hardware available to computer engineers and to organic evolution was also different, and in part determined the differences in architecture of successful brains and computers. Although the logic gate and the neuron have a great deal in common as we shall see, some of their differences turned out to have far-reaching consequences. The brain never had speed on its side, neurons operate in milliseconds not nanoseconds, but it never lacked for quantity. (You want million bit bytes and ten thousand legged gates? Sure, how many trillion?) The computer engineers on the other hand were limited in quantity by the expense and difficulty of assembly of their components, which dictated designs that were hardware conservative. This was compensated by using the speed of electronic components to substitute for quantity. Thus, our computers emphasize small bytes and few registers, but achieve high data thruput with iterative reuse of these components at great speeds. Bus oriented design and other hardware conservative adaptations arise from these same considerations.

In contrast, parallel multiprocessor designs with hierarchical organization, which the brain uses with wild abandon, are only seen in the most primitive form in our current computers and computer networks. The brain also has no compunctions about freely mixing digital and analog computing elements, using each to best advantage where needed. Thus, the brain and the computer have each found a design best suited to the problems they are required to solve and the hardware available, albeit big brains can do some computer-like functions, poorly; and big computers can do some brain-like functions, poorly.

Curiously enough, both the brain and the computer seem to have settled on a single basic organization whether the device is large or small. We all know how a computer works in principle, although different machines differ in detail. The processor, the bus, the clock, memory, the IO interface, all are arranged according to the same basic plan in large machines and small. Similarly, the brain of the white rat in my laboratory is of the same design, basically, as the brain reading this page. All the same parts are included in both, and hooked up in the same way. The differences are in capacity and relative development of the parts. Brains are even more similar to one another than computers.

What I am suggesting is that the computer has developed an architecture that is optimized for logical and mathematical problems, but that that is not an optimal architecture if the problem is to display basic common sense, whether it can do Fourier transforms or not. Thus, our machines as presently configured are terribly inefficient at the kinds of problems brains solve easily, and prodigious feats of programming, vast amounts of memory and all the speed that can be mustered give us only the most trivial results.

I am not going to suggest that we try to build a hardware replica of the brain. We don't have the hardware or the knowledge yet. I would like to suggest however that if we are interested in approaches to a science of robotics, it would be very instructive to examine the only model of an intelligent machine that is available to us, and to try to identify principles of operation that could

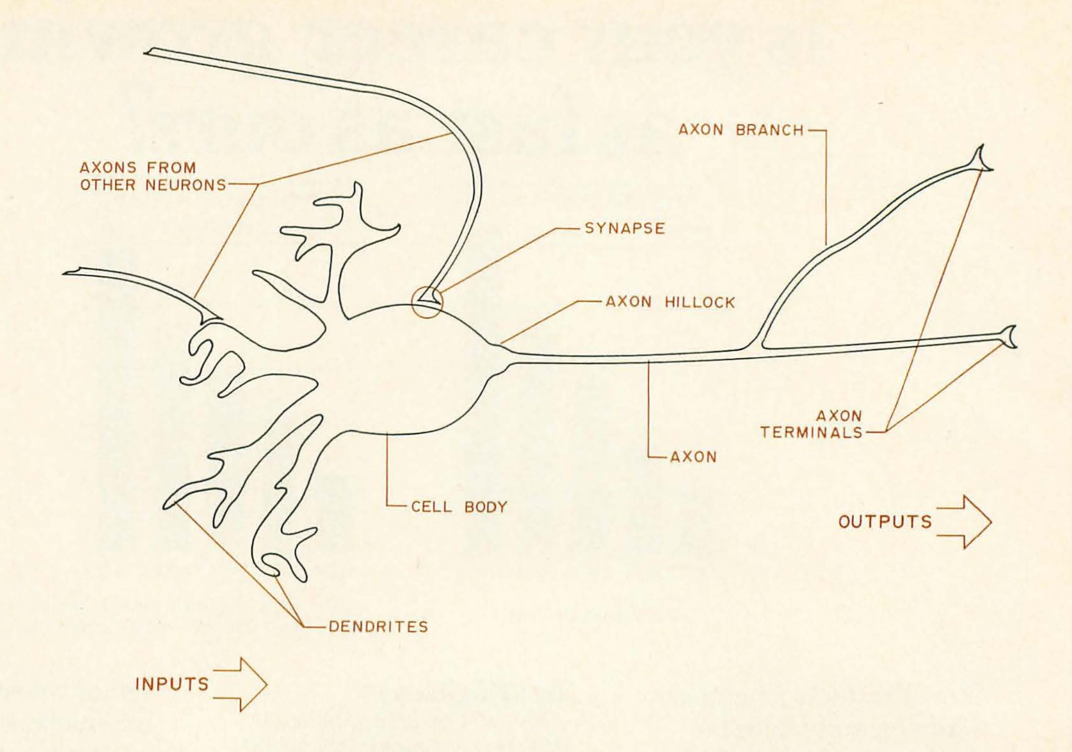


Figure 1: The parts of the neuron, the brain's basic "gate." Flow of information through this gate is roughly from left to right. Outputs are digital pulse streams transmitted through the axon and its branches to inputs of other neurons. Inputs are signals from other axons, which are summed by an analog process which weights various sources and fires an output pulse when a threshold is reached.

be put to good use with the kinds of hardware that we do have. This is a particularly appropriate time for such an exercise, since the hardware revolution has freed us to a degree from some of the original constraints upon computer design, and the growth of the computer hobby community has provided us with a group of eager experimenters who don't have a large investment in standard approaches, or a requirement to produce commercially useful business machines. Finally, our understanding of the operation of the brain has undergone something of a revolution in the last ten years, and we are in a much better position to discern the outlines of its architecture than we were when the computer was born. The time is right, the means are at hand, all we need are the geniuses in the basement workshops.

I am not going to tell you how to build a machine to work like a brain, because I don't know how. What I propose to do is to tell you, in terms of computer concepts, how a brain works. You supply the ideas from there. It is generally very difficult to explain brain operation to the layman, because he doesn't have the necessary concepts readily available. I have found, however, that it is very easy to explain brain operation to computer people because it can be translated into terms and concepts with which they are already familiar. If you can understand digital and analog electronics, you can understand in principle, if not in detail, how your brain works. You don't have to understand neurophysiology, neuroanatomy, neuropharmacology, and physiological psychology. (Well, maybe a little bit, but I'll try to keep it painless.)

First, you have to get a picture of the basic unit of brain structure. This is called a neuron. It is a cell like all the others in your body, but it is specialized for information processing. You can think of it as performing much the same function as a logical gate in a digital machine, or an operational amplifier in an analog machine. In fact, it is a very versatile device and can do either or both jobs. The brain uses neurons, billions and billions of them, to do everything it does. Let's look at the diagram of a neuron in figure 1. The output of the neuron appears on the long thin part labeled axon. Think of the axon as a wire. The brain uses them for transmitting information over distance. The difference is that this wire transmits only pulse streams, not DC levels. It's a



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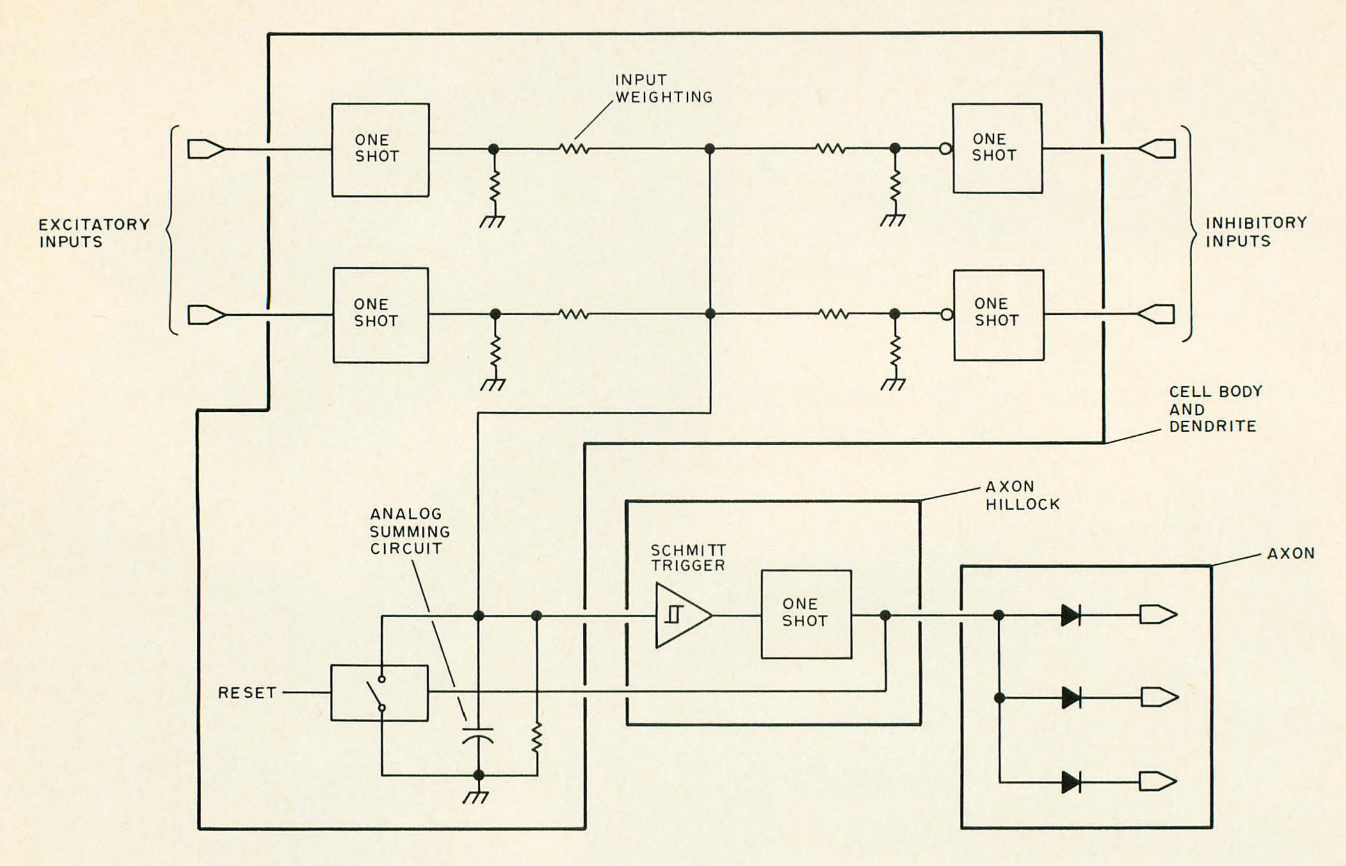


Figure 2: An equivalent circuit for the neuron, illustrating some of its important properties as an analog and digital device. This model should be compared to the information in figure 1.

digital wire. All the pulses are always the same height and duration, and can be thought of as binary bits. Only ones and zeros are allowed. Now look at the part labeled axon hillock. That's like a Schmitt trigger. It puts a pulse on the axon whenever the analog voltage in the part labeled cell body crosses a preset threshold value. Whenever this occurs, the voltage in the cell body is reset to the baseline or initial value. This cell body voltage is raised toward the Schmitt trigger's threshold, or dropped away from it, by the action of pulses impinging on the cell body from the axons of other neurons. The place where an axon meets a cell body is called a synapse, and it only transmits in one direction. Think of it as a diode. Now a synapse may be positive or negative. That is, a pulse at a given synapse may either add to or subtract from the cell body voltage. This is a function of which synapse receives the input, not the nature of the pulse (just like the little inversion circles on logic gate inputs). Remember however that the voltage in the cell body is an analog voltage and is performing an algebraic sum of the inputs. Moreover, the inputs may have different weights. The ones furthest from the axon hillock have the least effect, the ones nearest to it have the greatest effect. Weighting may be reduced greatly by placing the input far out on an extension of the cell body called a dendrite. The effect of an input outlasts the pulse that produces it, so that inputs which do not arrive synchronously in time may still sum within brief time limits. Think of it as a pulse stretcher at each input coupled with a time constant in the cell body. The effect of the finite time constant is to give each input pulse a temporal weighting (ie: the more recently arrived pulses have a greater weight in the sum).

When the inputs to the cell body have summed past threshold at the axon hillock, and a pulse has been placed on the axon as a result, we say that the neuron has "fired." An equivalent circuit (for our purposes) of the basic neuron is shown in figure 2. If you study figures 1 and 2 for a moment, you will see that the neuron has digital inputs, which are converted to analog values and operated on algebraically in an analog fashion. The result is then converted back to digital form for transmission. Now this is a very powerful tool. It can act as an AND gate (coincidence of several equally weighted inputs required to reach firing threshold), an OR gate (any

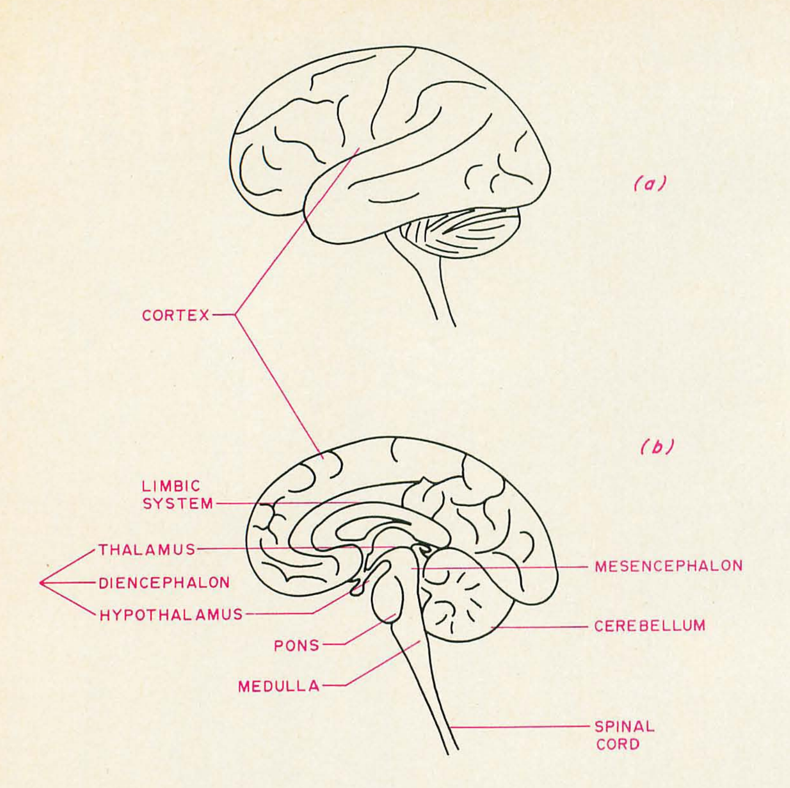
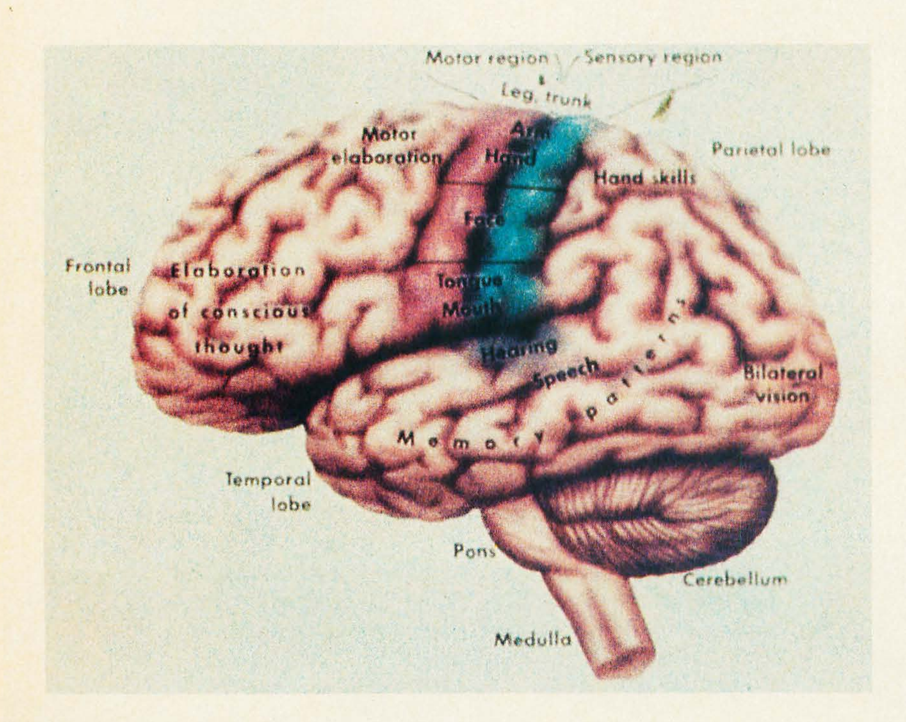


Figure 3: The brain as it appears anatomically. Above: a view of the brain from the left side. Below: A view from the left of the inside of the brain shown cut in half down the center line. The basal ganglia (striatum) which do not show here would be on either side of the thalamus.



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This illustration was supplied by the author.

of several inputs can drive the cell past firing threshold), or any of a variety of other functions (NAND and NOR can be achieved by cells with a resting potential above firing threshold, and inhibitory inputs). When you consider that one or more of the inputs to the cell can be feedback from its own axon, and that an average neuron may have ten thousand inputs, you begin to appreciate the possibilities. It can integrate and differentiate and do other useful functions by virtue of feedback and analog operation.

No one would try to design a very large system out of gates this complex unless someone finds a way to make them in quantity on a chip. Consideration of their operation however reveals some important considerations of brain architecture. First, although neurons can be synchronized by simultaneously driving them with an overriding input, they are normally asynchronous devices. The system can use local "clocks" where they are useful, but it doesn't have a system clock.

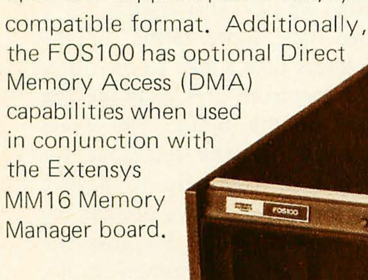
This permits an interesting development. In synchronous systems, information can only be coded in terms of which lines are active. If you want to indicate on or off status of some condition, you put a zero or one on the appropriate line. But if you want to indicate a numerical value greater than one, you have to do it by coding it as the activity, or lack of it, simultaneously on several lines. For example, we represent numbers by the bit pattern in a byte on the data bus. Now the brain can, and in several instances does, function in this mode. We refer to it as "place coding" because the information is contained in the location of the incoming signal. However, because it does not have to maintain synchronization, the brain can also encode information in terms of the frequency of arrival of pulses on the axon. We refer to this, obviously enough, as "frequency coding." Examination of the model circuit (figure 2) for the neuron reveals that the greater the positive input drive to the cell body, the more quickly the analog voltage will reach threshold, and the more quickly a new pulse will be placed on the axon after the reset following the preceding pulse. This means that it is very easy to use frequency coding to indicate the magnitude of the summed input activity. Due to the "pulse stretchers" at the inputs to the neuron, and the time constant of the cell body, pulses that are sequential on the axon can sum with one another to produce a greater analog voltage. This voltage is proportional to the frequency of the incoming pulses, and this achieves decoding of frequency coded input back to the analog mode.

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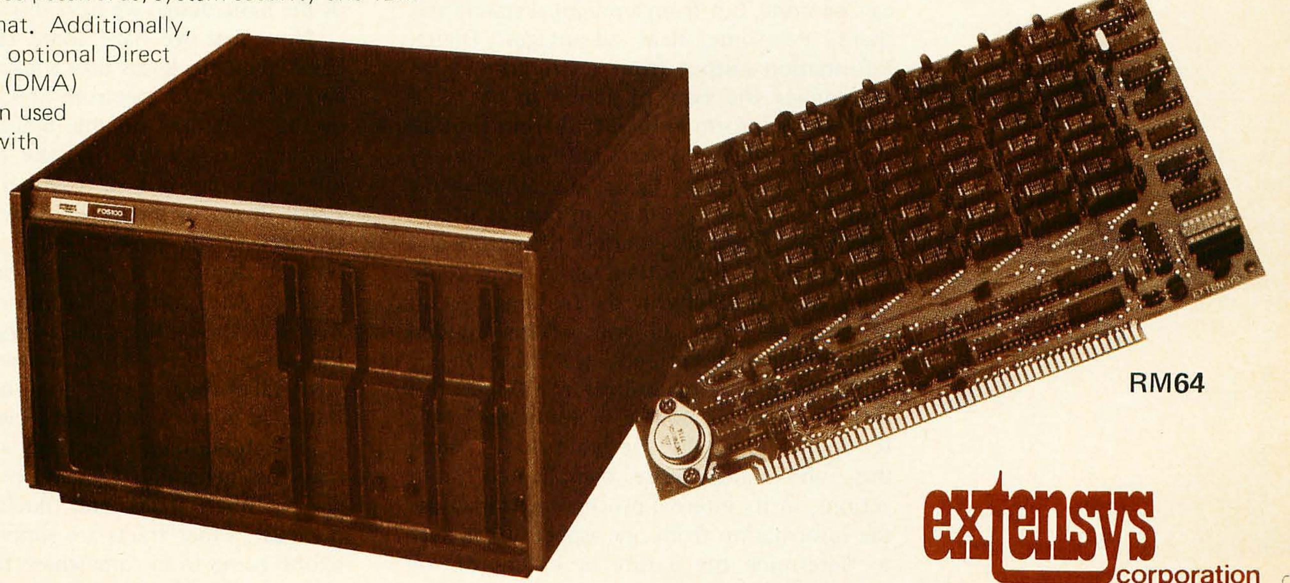
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Interaction of inputs from different axons is termed "spatial summation," and interaction of sequential pulses on the same axon is termed "temporal summation." One of the interesting things the brain can do with this capability is to use both place and frequency coding simultaneously on the same line. Another advantage is the ability to represent very large numerical quantities with what might be called a "temporal byte," or integration over a brief time period, of a single input line. As an example, consider the way the brain encodes sensory information from your skin. The type of sensation (ie: heat, cold, pressure, etc) as well as the location of the sensation is place coded. That is, *what* you feel is a function of which line is active. The magnitude of the sensation, *how much* you feel, is frequency coded on the same line. Thus, the brain structure receiving the information can determine the type and location of the stimulation with a "spatial byte," (place code) which determines the set of active lines, and the intensity of the stimulation with a "temporal byte" of frequency code.

The brain's basic "byte," therefore, has two dimensions, a spatial dimension and a temporal dimension. Two independent sets of information may be encoded in these two dimensions, and they may then interact in the receiving structure in a way determined by that structure. Notice that the spatial aspect of the byte is essentially digital information, and that the temporal aspect of the byte is essentially analog information, although it is encoded in the frequency of digital pulses.

The mathematical treatment of this is an information theorist's nightmare, although it can be done, but from a practical standpoint there are some clear advantages. Digital information output from a structure which determines the type of action to be taken and analog information output from another structure which determines intensity of action required may "gate" one another in a third location to produce an output stream which simultaneously defines the nature and magnitude of the action taken. One could think of it as specifying the enabling of a set of switches with an appropriately coded digital byte while presenting a set of analog values to the switched lines. We do see this sort of thing of course in some electronic IO applications, but the brain makes use of this, and much more complicated interactions, in its internal processing. It may use the information from one aspect of the byte to determine the nature or extent of the operation to be performed on the information in the other aspect of the byte.

Two additional properties of the neuron need to be mentioned to complete our understanding of the basic gate. The first is a different type of inhibitory input. The "negative synapse" described earlier puts an inhibitory input into the cell body to act on the analog sum there and retard the achievement of firing threshold at the axon hillock. This action of course simply antagonizes (with a specified weight) the action of all the positive inputs. Clearly, it does this without regard to which input it is antagonizing. It is also possible to have a "negative synapse" which antagonizes only a specific synaptic input. This is called "presynaptic inhibition," because it may be thought of as a disable input to one of the input one shots.

The final desirable property of the neuron as a computer element is that speed of transmission of pulses down the axon may vary over a wide range (although it is always the same in any given axon). This means that we may use high speed axons to move data quickly, but low speed axons may be employed as delay lines. Since axons can have branches coming off at any point, we may have tapped delay lines. We shall see some stunning examples of the utility of this feature.

It should be apparent by now that the basic neuron is an enormously powerful tool. In practice, few situations call for all of the complexity of this device, and it is frequently seen acting as simply a switch or AND gate or other very domestic sort of creature. Indeed, in many situations, neurons take on a variety of specialized shapes and connections which optimize them for one or another function, to the exclusion of others. In all cases however, their operation may be understood in terms of the basic design we have discussed.

Now that we have some terms for the basic elements, let us take a leap to the other end of the size spectrum and examine the overall structure of the brain. The exact anatomy is actually of little relevance for our purposes, but it may help to have a visual image of the device as we discuss the features of its parts. Figure 3 shows the general appearance of the human brain, together with some of its internal structure. Figure 4 shows the general organization of the parts as they would appear if the brain were taken out of the body, unfolded, and flattened out in a neat plan view.

The functional structures of the brain may be generally divided into two categories, fiber tracts and nuclei (plural of nucleus). Fiber tracts are simply bundles of axons going from somewhere to somewhere else, the cabling and wiring of the brain. The nuclei are groups of cell bodies. Each

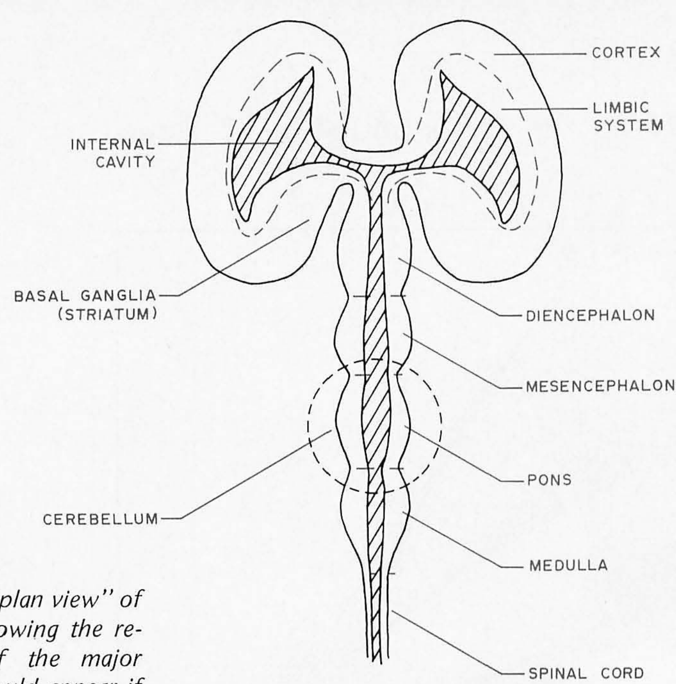


Figure 4: A "plan view" of the brain showing the relationship of the major parts as it would appear if it could be unfolded.

nucleus may be thought of as analogous to a central processor with a dedicated function, and (in most cases) a hardwired or ROM program. Most of the nuclei are irregular blobs of cell bodies, but in some cases the cell bodies are arranged in layers and the layers form a folded sheet of cells. In this case it is called a cortex rather than a nucleus, but the idea is the same. (The most famous of course is the cerebral cortex, of which humans are very proud because it is better developed in man than in most species.) The cells in the nuclei may be divided into two types: local neurons, whose function is in the data processing internal to the nucleus, and whose axons do not leave the nucleus, and output neurons which give rise to the axons that make up the fiber tracts and communicate with other nuclei. There are thousands of nuclei, of all levels of size and sophistication. Unfortunately, there is very little system to their names, and the names are either in Latin, or unpronounceable (Nucleus of Darkeschwitz, etc). The fiber tracts are bad too (Habenulointerpeduncular tract).

The only rational thing to do with the names of neuroanatomy is to endure them or ignore them. We shall try to ignore them. It will help however if you will take the time to learn the names of a few of the major divisions of the brain which are shown in figure 4 and to remember their basic relation to one another. The most important items, from bottom to top, are: the spinal cord, the medulla, the pons, the cerebellum, the mesencephalon, the diencephalon (and its two major subdivisions, the thalamus and the hypothalamus), the limbic system, the striatum, and the cerebral cortex.

This bottom to top sequence corresponds in a general way to a sequence of increasingly more global levels of control, from most detailed and specific, to most general and abstract. It also corresponds roughly to the evolutionary sequence from oldest and most primitive to most recent and advanced. All of the apparatus shown here is present by the time the evolutionary level of the mammals is reached.

The basic architecture of the system is hierarchical. Each of the major functions of the system is partially organized at each level of the system, rather than particular structures being devoted to particular major functions. At the lowest levels, there are a multitude of relatively simple processing elements doing similar jobs, and at the higher levels there are a few very complex and powerful processing elements defining system goals and priorities, and organizing the activities of the lower levels to achieve them.

On the input side, the lowest levels gather raw data which is then progressively abstracted, sorted and refined at each stage according to general guidelines which may be hardwired or provided by higher levels. The highest levels then receive abstract symbolic information about the general state of the environment rather than details. ("There is a black cat there" as opposed to "The following points of the visual field are dark.") Similarly, output functions begin at the highest levels, which determine general goals and strategies and transmit these in the form of statements about more limited momentary objectives to lower levels, which in turn send information about desired actions and timing to the lowest levels for execution.

Thus, at each level there are a number of relatively independent processing elements pursuing their own jobs in parallel real time, while trading information with echelons above and below, and laterally with one another. It follows that it doesn't make sense to ask where in the brain any large scale function is processed. Different aspects of it will be handled in different portions of functional subsystems which are represented at all major levels of the physical system. It might sound hopeless to try to follow the operation of such a device, but in practice there is order, not chaos. At the lower levels where semi-independent processors are most numerous, there is least diversity among them. The organization is in many ways like a military command chain, and one doesn't

Continued on page 96

UP AND RUNNING

TDL EQUIPMENT USED BY NEW JERSEY PUBLIC TELEVISION
TO PROCESS NEW JERSEY GUBERNATORIAL PRIMARY ELECTION RETURNS

John Montagna, computer engineer (above left), lead this successful network team in generating election results speedily, efficiently and reliably using predominantly TDL hardware and software. Montagna created three programs to get the job done. The text for a SWAPPER program was written and assembled using the TDL TEXT EDITOR and Z80 RELOCATING MACRO ASSEMBLER. The SWAPPER text and all debugging was run through TDL's ZAPPLE MONITOR. The relocatable object code was punched onto paper tape. A MAIN USERS program updated votes and controlled air display. An ALTERNATE USERS program got hard copy out and votes in. The latter two programs were written in BASIC. Montagna modified the ZAPPLE BASIC to permit time-sharing between the two USERS programs.

Four screens were incorporated, two terminals entered votes as they came in and were used to call back votes to check accuracy. Montagna called on the power and flexibility offered by TDL's ZPU board and three Z-16 Memory boards.

Montagna's setup worked constantly for over four hours updating and displaying state-wide and county-wide results without flaw.

"I chose TDL because they have all the software to support their hardware, and it's good; it has the flexibility to do the job."
John Montagna

We salute John Montagna and NEW JERSEY PUBLIC BROADCASTING for spearheading the micro-computer revolution.

TDL's XITAN SYSTEMS have the capacity to do similar tasks for you. Write to us for XITAN information and the name of your nearest TDL dealer.



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PRINCETON, NEW JERSEY 08540 (609) 921-0321

Circle 107 on inquiry card.



Seven points to consider before you buy your small computer.

In this magazine, alone, there are probably a dozen ads for small computers. New companies are breaking ground like spring flowers.

How, then, do you determine which computer offers the features you need most... at the price you can afford?

We'd like to propose seven basic questions to help you make an intelligent decision.

1. How complete is the computer system?

Many buyers of small computers are in for a rude awakening when they have to spend additional money for interfaces.

The Sol-20 Terminal Computer was the first *complete* small computer system. Everything you need to make it work is included in the basic package.

2. Is powerful system software available?

It won't do if your system is "tongue-tied."

Processor Technology Corporation has devoted more effort to the development of software than any other small computer maker. Our latest offering is the first fully implemented disk operating system for a small computer: PTDOS. It contains over 40 major commands, several languages and numerous utilities. Our high level languages include Extended BASIC, Assembler, FORTRAN,* FOCAL and PILOT.*

3. Is the system easy to expand?

More and more computer owners are expanding their small computers to handle business and other specialized requirements.

The largest Sol system can handle 64K bytes of RAM memory and operate with a three megabyte on-line disk memory. Sol systems use the S-100 Bus. So you can use a wide variety of hardware.

*Available soon.

4. Is the computer well-engineered?

Our Sol systems are the most conservatively rated and ruggedly built in the industry, period. In addition we designed them with you, the user, in mind; Sols are easy to build and a joy to operate.

5. Does it have proven reliability?

What is the track record? There are over 5,000 Sol systems in the field. Our track record for reliable performance is unparalleled in the small computer field.

6. Does it have good factory support?

A computer is a complex piece of hardware. So you want to be sure it is backed up with complete manuals, drawings and a factory support team that cares.

Processor Technology offers the most extensive documentation of any small computer manufacturer. And we maintain a patient, competent telephone staff to answer your questions.

7. Are maintenance and service people accessible?

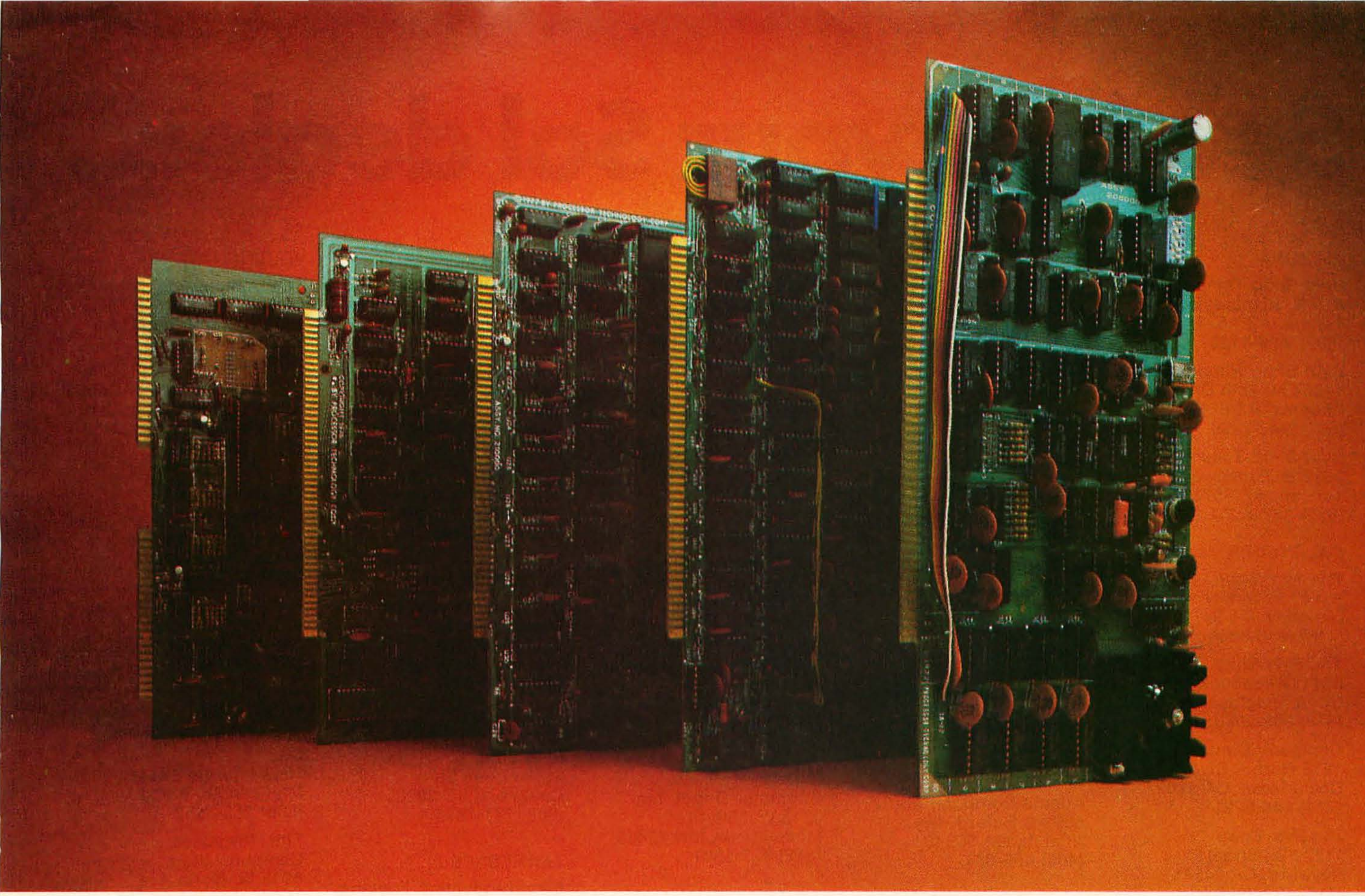
Where are they located?

Processor Technology has maintenance and service people in over 50 cities around the U.S.

As you continue turning the pages, see how we stack up to the other computers in this magazine. If we've succeeded in whetting your appetite, see your Sol dealer or write for information on the complete family of Sol computers.

Processor Technology Corporation, Box B, 7100 Johnson Industrial Drive, Pleasanton, CA 94566. (415) 829-2600.

Processor Technology



Subsystem B

Each board is a standout. Together, they're a powerhouse.

In the beginning there were boards, thousands of them.

That's how we started in the business. Making memories and interfaces for other people's computers…and making them better.

Now that our own Sol has become the number one small computer, you might think we're putting less emphasis on our board business.

Not so.

We're just doing more creative things with them.

One neat package gets your computer on the air.

For example, we've built Subsystem B, which ties together five Processor Technology modules into a completely integrated system that makes other S-100 Bus computers work almost as well as our Sol.

Subsystem B includes a memory module, three input/output modules, a general purpose memory, and appropriate software.

A specialized software program called CUTER knits together your computer and its peripherals to create an integrated, smoothly working system.

It's the fastest, cleanest way to get on line, and it costs less than if you bought each module separately.

You get your choice of two low power, reliable memory modules in 8K or 16K capacity.

Our VDM-1 video display module (still $199 in kit) is the industry standard display device with over 6,000 in use.

Our CUTS high speed, low cost ($110 in kit) audio cassette interface is the most reliable on the market and is supported by our broad line of cassette software including Extended BASIC, FORTRAN,* PILOT,* FOCAL and numerous others.

And our 3P+S input/output module offers a low cost way to handle virtually all the I/O needs of any S-100 Bus compatible computer system. There are close to 10,000 in the field. Price is just $149 in kit.

Yes, we may have become the maker of the Number 1 small computer — the Sol. But we haven't neglected the quality of our board business. We can't afford to… because we use many of them in our own computers.

For our most recent literature and price list see your dealer or write Processor Technology Corporation, Box B, 7100 Johnson Industrial Drive, Pleasanton, CA 94566. (415) 829-2600.

Processor Technology

*Available soon.

The IRS and the Computer Entrepreneur

Elizabeth M Hughes
5831 Hillside Dr
Doraville GA 30340

Few computer hobbyists ever have enough money to put into expanding, upgrading or otherwise improving their systems. New products for the home computer are appearing almost daily and new needs ("If I only had another 4 K of memory. . .") become visible as the computer receives increased use. It's hardly surprising, then, that many small-systems owners are thinking of ways to make their computers pay for themselves. Many succeed in penetrating the chinks in the armor of the local business community (or whatever) and begin to earn some money from the enterprise.

The ecstasy of turning a dollar from a hobby activity is hard to beat, but after that first burst of excitement, it's necessary to remember the cloud on the horizon: the Internal Revenue Service (IRS), which is interested in *all* earnings. The purpose of this article is to acquaint you with the additional tax schedules you must prepare and records you must maintain if you start earning money with your computer. On the brighter side, it will also give you an idea of the deductions you can take on the strength of your new status as a small business.

Tax law is complex, however, and an article of this length can only offer a thorough overview of the situation. Anyone starting a small business would be well-advised to augment the information presented here by getting the free IRS publications on the subject which are listed at the end of this article.

Are You a Small Business?

In deciding whether or not you are a "small business" for federal income tax purposes, the main considerations are (a) did you earn any money from the enterprise in question during the past year?; and (b) do you want to take deductions based on your status as a small business? If you take business-based deductions, your business can be a comfortable tax loss, but only for a short time. If you do not produce a taxable profit during at least two of every five consecutive years, you do not qualify as a business, in which case you may find yourself in the uncomfortable position of having claimed deductions in previous years from a nonexistent business. Therefore, unless you seriously intend to expand your money earning computer activities to the point of making a net profit, it's wise to simply report computer income under *miscellaneous income* on your regular tax form and leave it at that.

Other considerations arise on a state or local level. Before you decide to become a small business, be sure to find out what's involved in your area. Zoning ordinances in some cities render even in-the-home businesses illegal in certain areas. Some cities and states require an annual licensing fee from *all* small businesses, and state law varies radically regarding which goods or services are subject to sales tax. Inquiring into these matters at the outset will prevent problems later. In most areas, small businesses are not required to incorporate or to register their trademarks, if any (although they are permitted to do so); but all states and some municipalities have laws regarding small businesses which must be taken into consideration. Telephone calls to state and local government offices will usually answer these questions efficiently.

Satisfying the IRS

New small businesses, especially if they are responsible for tax losses in their first

The ecstasy of turning a dollar from a hobby activity is hard to beat, but after that first burst of excitement, it's necessary to remember a cloud on the horizon: the IRS.

New small businesses, especially if they are responsible for tax losses in their first year or two, are prime targets for IRS audits.

year or two, are prime targets for IRS audits. The thought of being audited by the IRS strikes terror into even the most innocent hearts, but if you keep complete and accurate records you can face even that contingency with unruffled calm.

The general rule is *keep everything.* In detail, this translates into keeping all receipts for business expense, paying as many business expenses by check as possible to provide the additional documentation of a cancelled check, and keeping thorough records of all income from your business. Remember that the IRS is always looking for falsified records of all sorts and has no reason to suppose that you haven't been doing the same, so *don't* rely on your computer printout or handwritten records to satisfy them. All those odd sized receipts may be a pain to keep, but if you're audited, they'll save the day.

Records needed fall into three categories: income, outlay and miscellaneous. Income records serve as the basis for calculating your total business income at tax time. For example, if you bill someone for a computer service, keep a copy of the invoice you send out and note on it such particulars as date, service, customer's name and address, and postage required to send the bill. When payment is received, mark the invoice with the date of payment and file a photocopy of the check with it. A record of the date of payment is especially desirable if you are paid in cash, and for this reason an inexpensive receipt book can be a worthwhile investment.

One successful business I know keeps records in paper bags, one marked "expense" and the other "income."

Records of outlay serve to document expenditures made for the business. They are especially important because they support any business deductions you claim at the end of the year. Anything purchased exclusively for business use is a safe deduction. Thus, if you buy a cassette which is used solely for business data (as opposed to programs for your private amusement), it counts as a business expense; but if you buy a sheet of stamps, you can only count as business expense those stamps used for business purposes, such as mailing bills or advertising.

Miscellaneous records document your claim to be a business. They include copies of any advertising you do, business correspondence, and announcements (or newsclips) of activities you participated in which mention that you are the proprietor of your business.

The central fact to remember is that the IRS takes nobody's word for anything and looks at any record with a critical eye. Fraud and conspiracy to defraud are ever present, and the IRS is continually on guard against them. Therefore, any record which involves a business other than your own (eg: the company you bought *x* from), a bank, or another individual (a customer, a news reporter, whatever) helps your cause by providing someone who can attest to your business activities. All of this inevitably sounds paranoid, but a little well-placed forethought and paranoia can save trouble later.

Getting Organized

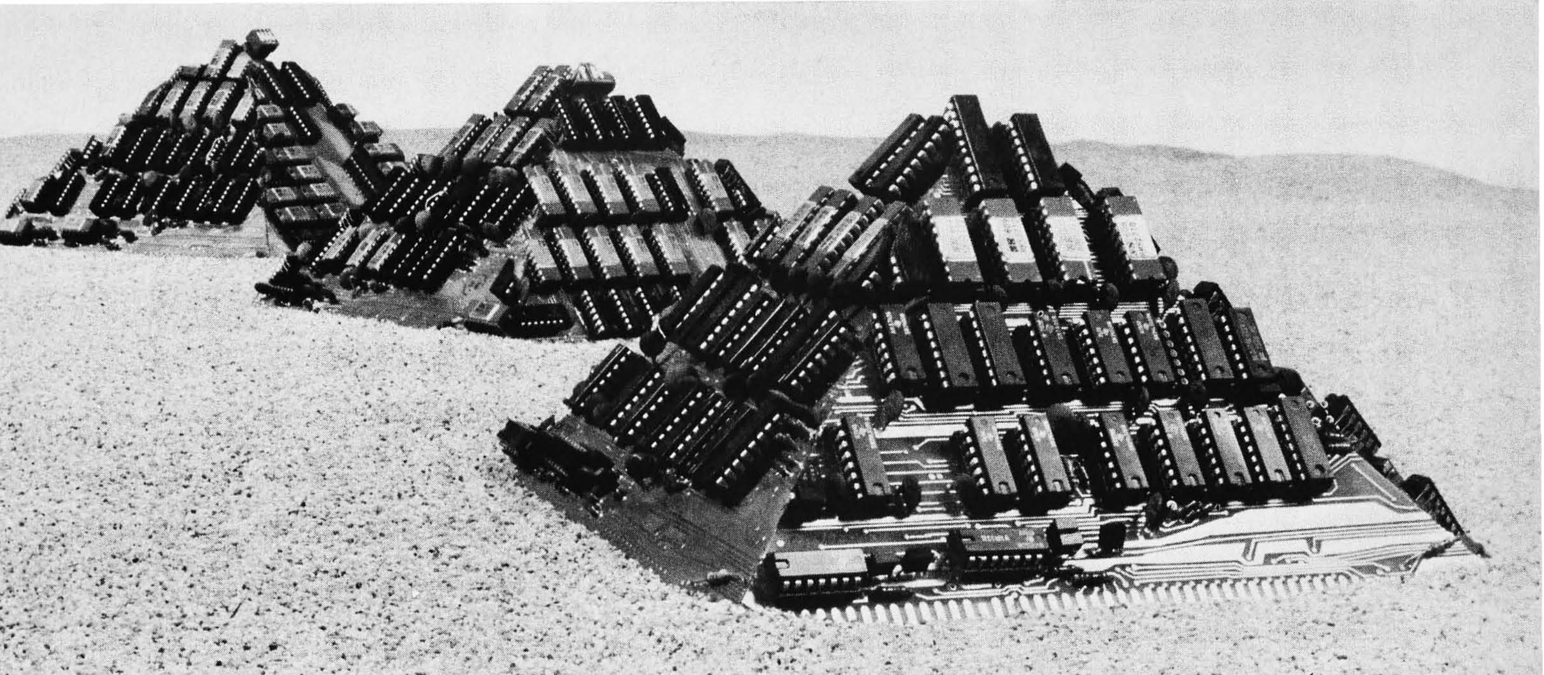
Naturally, all these documents amount to a lot of paper, usually in odd sized scraps that have the knack of vanishing at inconvenient moments. There are several approaches to making life easier at tax time. One successful "small business" I know uses paper bags. The entrepreneur of this enterprise keeps one marked *expense* and one marked *income* by the desk and pitches all documents into one or the other. When preparing tax forms, he sorts the bags, combining related documents into rubber-banded bundles, and, after the forms are mailed, puts all the documents plus a copy of the tax forms into one large paper bag. Stapled shut and labelled with the year, it then takes its place among previous years' bags on a shelf as insurance against the day the IRS decides to audit.

I personally prefer a somewhat more complicated system employing file folders. Each client or type of expense has its own file folder which I can use not only for tax purposes but as a basis for estimating anticipated needs. If the money can be available before the expense arises, life is made easier; and if a service can be offered to a client just as he/she is about to request it, business flows more smoothly.

Regardless of system, however, the principle is the same: keep hard copy proving the legitimacy of every deduction and every bit of claimed income. Try different approaches until you find the one that suits you best, and then stick with it. It's your best defense against allegations of tax fraud.

The Silver Lining

If all this sounds like a lot of trouble, you're right. But it has advantages. And in the language of income tax, "advantage" is spelled *deduction.* Small business expenses are deductible. What counts as a business expense? Schedule C, the main tax form businesses must fill out (more about this later), lists several categories. Let's consider them one by one.



The cost of replacing a 2102 programmable memory which gave up the ghost is deductible as a repair cost, but upgrading it to a 2102-1 or adding another 4 K bytes of memory to the system is an improvement and must be treated differently.

Depreciation

If you buy any income producing property or property used in your business which has a limited useful life that can be reasonably estimated, you may, during the years of its useful life, recover some of its cost in the form of depreciation. If, for example, you buy an item to use in your business that will wear out or need replacement in time, you can deduct a certain percentage of its cost every year of its estimated life. If you are using the item for nonbusiness as well as business purposes, you may only deduct the depreciation for the period of business use. Thus, if you buy a computer which will be used one third of the time for business and the other two thirds of the time for nonbusiness uses, only one third of its annual depreciation can be deducted as a business expense.

There are many ways of calculating depreciation. Tax law surrounding it is too complicated for thorough discussion in an article of this length, but since much of the expense of a small computer business arises from purchases of depreciable property, it is well worth a detailed study if you start your own computer-oriented business.

Taxes on Business and Business Property

This includes tax on business property (if you conduct your business on land you own and on which you must pay property tax); personal property tax, sales tax, gasoline tax, and the like if they were incurred in the ordinary course of business; state imposed corporate franchise tax; and, if you have employees, employment taxes. Of these, only sales tax (in applicable states) and gasoline tax are apt to be worth the computer entrepreneur's time as deductions, but be sure to deduct all that apply and are documented.

Other Business Property Deductions

If you rent an office from which you conduct your business, the rent is deductible. If you operate from your home, however, you get no such deduction except under very special circumstances which are discussed in greater detail below. Unless you are engaged in your business full time, however, attempting to get this deduction will almost certainly be more trouble than it's worth.

Routine repairs and maintenance of business property (the office, if any, the computer, etc) are deductible only if they do not increase the value, utility or life expectancy of the repaired item. Thus, the cost of replacing a 2102 programmable memory which gave up the ghost unexpectedly is deductible as a repair cost, but upgrading it to a 2102-1 or adding another 4 K of memory to the system is an improvement and must be treated differently.

If you carry business insurance, the premiums are deductible.

Salaries, Wages, and the Like

If you have employees, there are deductions for salaries, wages, commissions and numerous forms of employee benefits, but you may not deduct any salary, wage or compensation paid to yourself. If you claim deductions in these categories, be prepared to prove that the service paid for (eg: date entry) actually was rendered, that the payment for the service actually was made, and that the rate of pay was reasonable.

You may also deduct the fees of lawyers, accountants and the like whose services your business uses.

Financial Business Deductions

You may claim deductions for bad debts arising from sales or services, for interest on loans made for or by the business, and for a number of other more complex financial matters which arise from certain business tax breaks. Unfortunately, computer entrepreneurs are not likely to qualify for the tax breaks, so I merely mention their existence in passing.

Other Business Expenses

Most of your deductions are apt to fit into this category. If you're renting an office, you can deduct the costs of heat, light, telephone and trash removal. These are also deductible if you qualify for a deduction for conducting business in your home, but in any event you can safely deduct business long distance telephone calls. The cost of postage is deductible for all business correspondence including mailed advertisements and bills, as is any paper and printing expense which you incur for your business. Similarly, your investment in receipt books, file folders and other supplies used to maintain tax records is deductible.

One of the largest deductions of the computer entrepreneur will probably be for reference and research materials. If you purchase books or magazines which give you information which contributes to the success of your business (eg: an issue of a magazine containing a program for a service you subsequently sell), the cost of the publication is a deductible expense. Memberships in professional societies, subscriptions

Price/Performance no one else has put together.

IMSAI Introduces the PCS-80/30 Integrated Video Computer

- ☐ 3 mHz microcomputer
- ☐ 3K ROM monitor
- ☐ 2K RAM
- ☐ 8 expansion slots
- ☐ 14 mHz integrated intelligent CRT (24 x 80)
- ☐ Intelligent Keyboard
- ☐ Parallel interface
- ☐ 2 serial interfaces
- ☐ Graphic and edit CRT functions
- ☐ 28 amp power supply
- ☐ All for **$1499*** assembled and tested.

Software:
ASSEMBLER, DOS, TTY and ACR BASIC, Commercial/Scientific BASIC, FORTRAN IV and more.

Memory Options:
4, 16, 32 and 64K RAM memory boards.

Circle 51 on inquiry card.

Peripherals:
Printers, floppies—mix and match; standard, mini and high performance double density floppy disks on the same system (an industry first), ½″ magnetic tape drive, CRT and TV monitors.

Send today for your copy of the 250-page IMSAI PCS-80/30 User Manual. Price $5.00. The cost of the manual may be applied towards your purchase of a PCS-80/30 Integrated Video Computer. Use the coupon provided.



Gentlemen:
Send me the IMSAI PCS-80/30 User Manual, price $5.00. I understand that the $5.00 may be applied towards the purchase of a PCS-80/30 Video computer System.

Check/Money Order enclosed. Amt. $________
Charge my ☐ BAC ☐ M/C

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*U.S. domestic price only. PCS-80/30 kit available. Other PCS-80 kits start at $699. Prices and specifications subject to change without notice.

to technical journals, the automotive expense incurred by your business, and books and business equipment having a useful life of less than one year can also be deducted.

A lot of things suddenly become deductible when you're a small business, with the result that care and good judgement are even more necessary than usual in filling out your tax forms. If you have any doubt about the legitimacy of a deduction or your ability to substantiate it, don't take it. In fact, the first year you file as a small business it's wise to go easy on everything while you become accustomed to the forms and laws. Then, as you grow more familiar with the ins and outs of tax for small businesses, you'll be able to claim more of your deductions with the certainty that, should you be audited, you'll be able to support them adequately. Let's look at the additional tax schedules you'll need to fill out.

Schedule C (Form 1040)

This is the main schedule you'll have to worry about. Figures 1 and 2 show the front and back of the 1976 Schedule C, respectively. They have been filled out with the tax information on a fictitious computer entrepreneur. You can follow them through the discussion below.

At the top of figure 1 is a place for your name and social security number. This provides cross-indexing to your Form 1040, filed simultaneously. Below, in A through H, you indicate the general shape of your business: (A) what you do and produce, (B)

Figure 1: Schedule C, "Profit (or Loss) From Business or Profession."

SCHEDULE C (Form 1040) Department of the Treasury Internal Revenue Service

Profit or (Loss) From Business or Profession
(Sole Proprietorship)
Partnerships, Joint Ventures, etc., Must File Form 1065.
► Attach to Form 1040. ► See Instructions for Schedule C (Form 1040).

1976

Name of proprietor: F. J. WINSTEAD — Social security number: *** | ** | ****

A Principal business activity (see Schedule C Instructions) ► COMPUTER SERVICES; product ► PROGRAMS, PRINTOUTS, ETC.
B Business name ► WINSTEAD COMPUTER SERVICES — C Employer identification number ► NONE
D Business address (number and street) ► #124 HIGH LAWN TERRACE BUILDING
City, State and ZIP code ► COMPUTERVILLE, USA *****

C

	Yes	No
E Indicate method of accounting: (1) ☑ Cash (2) ☐ Accrual (3) ☐ Other ►		
F Were you required to file Form W-3 or Form 1096 for 1976 (see Schedule C Instructions)?		✓
If "Yes," where filed ►		
G Was an Employer's Quarterly Federal Tax Return, Form 941, filed for this business for any quarter in 1976?		✓
H Method of inventory valuation ► NO INVENTORY. Was there any substantial change in the manner of determining quantities, costs, or valuations between the opening and closing inventories? (If "Yes," attach explanation)		

		Line	Amount	¢
Income	1 Gross receipts or sales $ 254.97 Less: returns and allowances $ 0.00 Balance ►	1	254	97
	2 Less: Cost of goods sold and/or operations (Schedule C-1, line 8)	2	20	64
	3 Gross profit	3	234	33
	4 Other income (attach schedule)	4	0	00
	5 **Total income** (add lines 3 and 4)	5	234	33
Deductions *	6 Depreciation (explain in Schedule C-3)	6	0	00
	7 Taxes on business and business property (explain in Schedule C-2)	7	0	00
	8 Rent on business property	8	419	04
	9 Repairs (explain in Schedule C-2)	9	0	00
	10 Salaries and wages not included on line 3, Schedule C-1 (exclude any paid to yourself)	10	0	00
	11 Insurance	11	0	00
	12 Legal and professional fees	12	0	00
	13 Commissions	13	0	00
	14 Amortization (attach statement)	14	0	00
	15 (a) Pension and profit-sharing plans (see Schedule C Instructions)	15(a)	0	00
	(b) Employee benefit programs (see Schedule C Instructions)	(b)	0	00
	16 Interest on business indebtedness	16	0	00
	17 Bad debts arising from sales or services	17	0	00
	18 Depletion	18	0	00
	19 Other business expenses (specify):			
	(a) HEAT AND LIGHT — 54.71			
	(b) TELEPHONE (INCLUDES BUSINESS LONG-DIST.) — 40.15			
	(c) POSTAGE — 19.13			
	(d) TRASH REMOVAL — 15.84			
	(e) REFERENCE/RESEARCH. BOOKS, MAGAZINES — 107.22			
	(f) MEMBERSHIPS - PROFESSIONAL SOCIETIES — 30.00			
	(g) ADVERTISING - PRINTING — 25.77			
	(h) BUSINESS AUTOMOTIVE EXPENSE — 29.20			
	(i) SUPPLIES - TAX RECORD BOOKS, FILE FOLDERS, ETC. — 5.86			
	(j) SUPPLIES - CODING PAPER, ETC — 19.26			
	(k) Total other business expenses (add lines 19(a) through 19(j))	19(k)	345	28
	20 **Total deductions** (add lines 6 through 19(k))	20	764	32
	21 Net profit or (loss) (subtract line 20 from line 5). Enter here and on Form 1040, line 29. ALSO enter on Schedule SE, line 5(a)	21	− 529	99

BE PREPARED TO INCLUDE (AND PREFERABLY INCLUDE) ITEMIZED LISTINGS WITH DATES, ITEMS, AND AMOUNTS TO EXPLAIN ALL 19A-J AMOUNTS.

SCHEDULE C-1.—Cost of Goods Sold and/or Operations (See Schedule C Instructions for Line 2)

	Line	Amount	¢
1 Inventory at beginning of year (if different from last year's closing inventory, attach explanation)	1	0	00
2 Purchases $ ..... Less: cost of items withdrawn for personal use $ ..... Balance ►	2	0	00
3 Cost of labor (do not include salary paid to yourself)	3	0	00
4 Materials and supplies PRINTOUT PAPER $7.53; RIBBONS $5.02; CASSETTES $8.09	4	20	64
5 Other costs (attach schedule)	5	0	00
6 Total of lines 1 through 5	6	20	64
7 Less: Inventory at end of year	7	0	00
8 Cost of goods sold and/or operations. Enter here and on line 2 above	8	20	64

Did you claim a deduction for expenses of an office in your home? ☐ Yes ☐ No

* TO AVOID THE POSSIBILITY OF SOMEONE TAKING HYPOTHETICAL DEPRECIATION ON AN ITEM AS A BASIS FOR THEIR DEPRECIATION, NO DEPRECIATION IS CLAIMED HERE.

the name under which you do it, (C and D) address, (E) accounting method, (H) inventory evaluation method, and (F and G) two bits of information you don't have to worry about unless you have employees. If you're selling a hardware item, you'll need to evaluate your inventory, if any, but as most computer entrepreneurs sell computer services, we'll leave that question for those who sell hardware to examine. The computer entrepreneur with paid employees is rare, so we can assume that in most cases both F and G can be marked "No."

The *accounting method* you choose in the beginning is the one you'll be stuck with forever, unless you file a request to change it with the IRS. If you choose a method other than "cash" or "accrual," that also must be cleared with the IRS, so most people select one or the other of the more commonplace methods. The difference between the two methods hinges on when you can claim deductions, etc. In the accrual method, payments and bills are taken into account when they are *due*, not necessarily when the money changes hands. Thus, you can claim a deduction for a business expense which fell due in December on that year's taxes even if you don't get around to paying it until January. At the same time, if someone owes you money in December, you must pay your tax as if it had been received then, even if he/she doesn't get around to paying you until January (or June, for that matter). Using the cash method, bills and payments are taken into account when they are paid. Each method has its advantages and disadvantages, but I would recommend starting with the cash method because of its simplicity. When you can afford an accountant

Schedule C (Form 1040) 1976 Page 2

SCHEDULE C–2.—Explanation of Lines 7 and 9 ITEMIZE TAXES AND REPAIRS HERE

Line No.	Explanation	Amount	Line No.	Explanation	Amount
		$			$

SCHEDULE C–3.—Depreciation (See Schedule C Instructions for Line 6)
If you need more space, use Form 4562.

a. Description of property	b. Date acquired	c. Cost or other basis	d. Depreciation allowed or allowable in prior years	e. Method of computing depreciation	f. Life or rate	g. Depreciation for this year
1 Total additional first-year depreciation (do not include in items below) →						
2 Other depreciation:						
SEE NOTE AT BOTTOM OF FIG. 1						
3 Totals						
4 Less amount of depreciation claimed in Schedule C–1, page 1						
5 Balance—Enter here and on page 1, line 6						

SCHEDULE C–4.—Expense Account Information (See Schedule C Instructions for Schedule C–4)

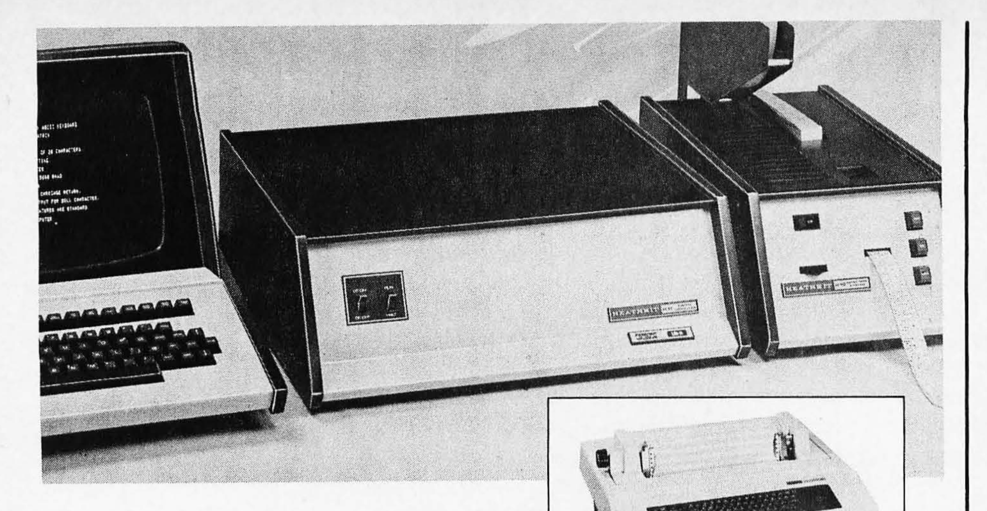
Enter information with regard to yourself and your five highest paid employees. In determining the five highest paid employees, expense account allowances must be added to their salaries and wages. However, the information need not be submitted for any employee for whom the combined amount is less than $25,000, or for yourself if your expense account allowance plus line 21, page 1, is less than $25,000.

Name	Expense account	Salaries and Wages
Owner		
1		
2		
3		
4		
5		

Did you claim a deduction for expenses connected with:
(1) Entertainment facility (boat, resort, ranch, etc.)? . . ☐ Yes ☐ No (3) Employees' families at conventions or meetings? . . ☐ Yes ☐ No
(2) Living accommodations (except employees on business)? ☐ Yes ☐ No (4) Employee or family vacations not reported on Form W–2? ☐ Yes ☐ No

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Figure 2: Schedule C, back view.





Fully assembled DEC Writer II Keyboard Printing Terminal at the sensational low price of only $1495!

Take an even BIGGER Byte!...

with the Heathkit H11 16-Bit Personal Computing System

Based on the world-famous DEC LSI-11, the Heathkit H11 and it's peripherals are designed to give you all the power and speed you need for total computing versatility. It's one of the few FULL 16-bit personal computers available to hobbyists today, and equivalent commercial versions would cost literally thousands of dollars more! As with the H8 system, complete "program-ready" software is supplied: the Heath/DEC PDP-11 software includes ED-11 editor; PAL-11S relocatable assembler; LINK-11S link editor; Absolute Loader; ODT-11X debug; IOX LP I/O executive program; DUMP-AB-PO and DUMP-AB-PB; plus BASIC and FOCAL; and it executes the PDP-11/40 instruction set! The software is supplied in easy-to-use paper tape format, perfect for the H10 paper tape reader/punch. And with Heath's complete assembly manuals and software documentation, you have the most solidly supported computer system you'll find anywhere. Sink your teeth into it today!

H11 LSI-11 16-Bit Computer	**$1295**
H11-1 4K Memory	**275**
H11-2 Parallel Interface	**95**
H11-5 Serial Interface	**95**
H10 Paper Tape/Reader/Punch	**350**
H36 LA36 DEC Writer II	**1495**
If purchased separately,	**$3605.00**

Heath System Price $3350.00

Prices are mail order net F.O.B., Benton Harbor, Michigan.
Prices and specifications subject to change without notice.

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Los Angeles, 90007
2309 S. Flower St. 213-749-0261
Pomona, 91767
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2001 Middlefield Rd. 415-365-8155
Sacramento, 95825
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Chicago (Downers Grove, 60515)
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E. Detroit, 48021
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to handle such matters, he/she can arrange to change methods if it becomes desirable.

The section labelled income comes next. The total received by your business for sales of products and/or services goes on line 1. You may subtract from it any money lost through returned items, rebates and the like, but these aren't apt to arise in this business. Before completing the rest of this section, look at Schedule C-1 at the bottom.

Line 1 of Schedule C-1 lists beginning of year inventory. If you're dealing in services, this should be 0, and H (at the top) should be "no inventory." Line 2, similarly, will be 0, since you haven't bought any items to add to a nonexistent inventory. Cost of labor (line 3) will also probably be 0, since you can't include your own salary or wage and you probably don't have any other employees. Only lines 4 and 5 are likely to contain anything. *Materials and supplies* are the costs of the tapes, etc, on which you store a customer's data; the paper on which you write programs; the printout paper you use to output hard copy either during a run or to give the customer; the ribbon on your hard copy output device; and anything else in the way of purchased materials that is required for producing the service and/or hard copy you provide the customer. To play it safe, I always include here only documentable purchases of supplies made during the tax year and spell out the items and their prices so the total will make sense. On line 5 (*other costs*), show such costs as overhead expenses (eg: the cost of running the computer) and shipping costs (if you have to mail someone a printout, for example). I routinely leave line 5 blank, since it's easier to figure these costs with the other expenses of the same type under *other business expenses* (line 19). Total lines 1 through 5 to get line 6. Since you have no year-end inventory, line 8 should equal line 6.

Now enter the total shown on line 8 of Schedule C-1 on line 2 and subtract. Line 3 in the income section is then gross profit. Miscellaneous income if any (recovered bad debts, interest on business investment, etc) is line 4, and line 5 shows the total business income for the year.

The section marked deductions (lines 6 through 20) comes next. *Depreciation* (line 6) is calculated and explained in Schedule C-3 on the other side of Schedule C. Deductions for repairs (line 9) and tax on business property (line 7) are similarly itemized in Schedule C-2. Both depreciation and the other deductions mentioned in lines 6 through 19 have been discussed above, but an examination of the deductions shown in lines 19a through 19j in figure 1 might be instructive. Line 19k, of course, is simply the total of these "other" expenses, and line 20 is the total of all business deductions.

You can always deduct the postage and telephone expenses your business involves. If you mail out a bill, an advertisement or a prospectus for your business, keep a record of the actual postage amount it requires. The IRS isn't interested in how many stamps you bought or an approximate figure. You must show dollars and cents actually spent for the business and nothing else. Unless you mail all business correspondence from a post office, getting a receipt for your stamps every time, this is a very hard deduction to document, but it can prove worth the effort since, with continually increasing postage costs, a business can involve a sizable postage expense. Similarly, if you make long distance telephone calls for your business, they are deductible and your phone bill and cancelled check can provide some of the necessary documentation. Keep a record of the business phone calls you make, showing the date, the number called, what person or company was reached at that number for business purposes, and a rough note of the purpose of the call and the length of time it involved. This is particularly important if you're doing business by long distance telephone with a friend or a member of your family, since the IRS will inevitably wonder how much of the call was business related.

Another item you can always deduct is any book, magazine or other work which you use as reference or research material. If the publication's business related information has a useful life of less than a year, then its price is fully deductible; if its usefulness exceeds a year it becomes a depreciable investment. For all practical purposes, it's rarely worth depreciating these references. In this field, information is apt to be outdated in a short time, so you might as well deduct the whole price the year you buy the publication. Be careful, though, to only deduct publications which contribute to your business, and keep the publication as evidence both that you bought it (along with the sales receipt) and that it is business related.

Advertising costs are also deducted here. This includes any expenses involved in preparing, printing and distributing advertising for your business. As usual, document the expenses as thoroughly as you can.

To keep all these records, record books, file folders and the like will be needed. These can be listed as supplies and their cost deducted here. Other supplies include any staples of your trade (tape cassettes, print-

Routine repairs and maintenance of business property are deductible only if they do not increase the value, utility, or life expectancy of the repaired item.

Continued on page 80



WANTED: MEDICAL APPLICATIONS

I have been reading your magazine with great interest. I would like contact with any of your readers who are interested in medical applications of computer technology, especially information on:

(1) Electrocardiogram interpretation and details on conversion, A/D, D/A, with appropriate interfacing for Z-80 processor.
(2) Software on any medical item especially diagnosis of endocrine, ovulation disturbances.
(3) Medicaid, Medicare, third party billing software.
(4) Business software.

Jonathan C Gibbs Jr MD
Catholine A Gibbs
Memorial Health Center
75 Harrison Av
Jersey City NJ 07304

NEEDED: PROSTHESIS CONTROLLED BY COMPUTER

I would like to pose a problem to my fellow readers. Recently someone I know suffered a broken neck. He will be paralyzed from the neck down for the rest of his life. All he can do at present is to breathe, talk, see, hear, and nod his head. Someone is supposed to have on the market a microcomputer controlled wheel chair that is run by a breath or voice actuated terminal. It is not hard to imagine a keyboard that can be played like a harmonica, with optical switches set with reeds mounted on diaphragms to act as SPDT momentary contact switches.

The problem is this: Given the current technology in motorized wheelchairs and electromechanical devices (such as articulated arms, spoon holders and page turners), develop a microcomputer operating system that can be entirely controlled from a breath activated terminal. The operating system should not only control the chair, it should allow the operator to call up all of the usual microcomputer operating systems, such as BASIC and assembler. If the operator chooses to become his own programmer, then he should be able to teach his chair new tricks as well as using the system for entertainment.

Remember also the limitations. A wheelchair can only carry so many batteries. The operator cannot afford to be stuck with an expensive, one of a kind, poorly documented and inflexible system; if he has a programming or hardware problem, he shouldn't have to go to a highly paid engineering consultant for a fix. If the wheelchair runs away, the operator can't get off; the system for operating the wheelchair should have enough checks and balances to prevent inadvertent injury.

With the advent of the hobby computer, the time is ripe for victims of amputation and paralysis to take more control of their lives.

Don Baker
Gloucester Pt VA 23062

You point out one of the most encouraging and heartening effects of research in robotics: application of this technology to improve the lives of severely handicapped people.

IBM 5100 PLUG INS, ANYONE?

We have an IBM 5100 32 K installed at our office. I have noticed many ads in your magazine for add on memory for other small systems, and wonder if anyone "out there" may have plug in memory cards to fit the 5100. I sure would like to hear from anyone who does.

AD Phelps
Hood River Distillers Inc
POB 240
Hood River OR 97031

NEEDED: INFORMATION ON COMPUTER CONTROLLED HYDRAULICS

I am an amateur computer hobbyist interested in computer controlled applications. I would like to know if you have any information on sources of miniature or small scale hydraulic components.

Peter Woodall
1645 DeMaisonneuve Blvd #609
Montreal, Quebec
CANADA H3H 2N3

We do not have any information on this subject, but perhaps a reader might care to provided a tutorial on the control of hydraulic systems from computer outputs. As a component of practical robotic systems, hydraulic technology might well be worth exploring.

TOWARD SMARTER MACHINES

Forgive me, but I feel a strong urge to comment on the statement made by Mike Rivers in the September 1977 BYTE [*Letters, page 180*].

When people take a particularly strong interest in a subject, they gen-

Continued on page 130

Ciarcia's Circuit Cellar

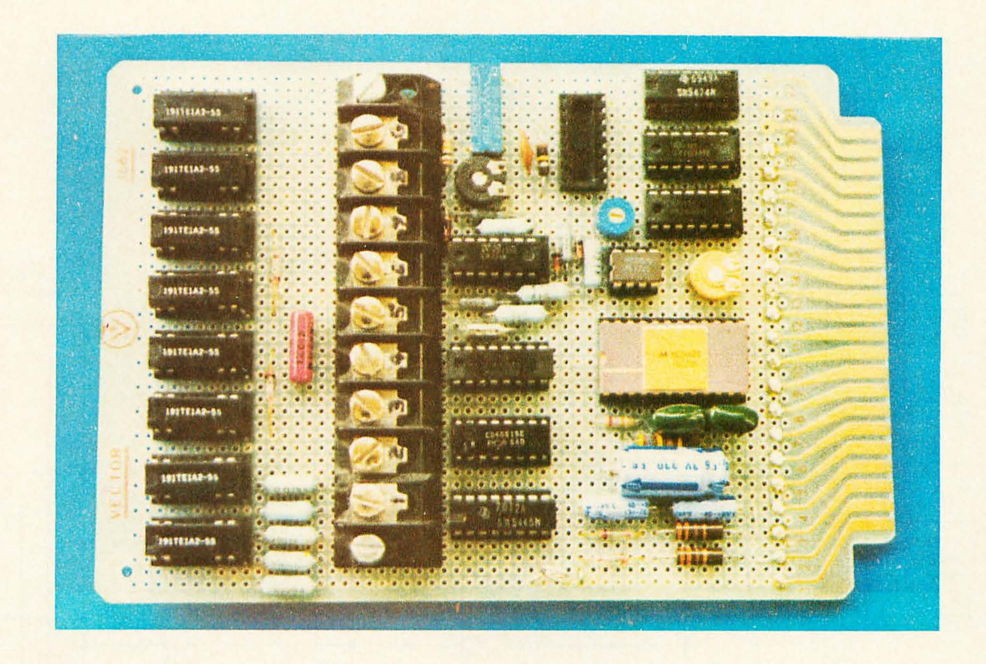


Photo 1: The prototype board for the expanded digital voltmeter.

Add More Zing to the Cocktail

Steve Ciarcia
POB 582
Glastonbury CT 06033

Last month (page 76) brought you a design for an 8 channel 3 1/2 digit 0 to 2 V digital voltmeter (DVM) interface. The article introduced multiplexed analog data acquisition by means of a construction project.

I'm sure that the majority of the readers who have built the DVM will be satisfied with the results. There is of course that small group of problem makers who don't believe the whole world exists in the range from 0 to 2 VDC: a point well taken.

Actually, I planned to expand the capabilities of the basic DVM all along. I'll elaborate in detail; the end result will be a DVM interface with these additional specifications:

Super Cocktail DVM

- 8 programmable input channels
- AC or DC capability
- programmable gain of 1, 10, or 100
- ranges of 0 to 200 mV, 0 to 2 V, 0 to 20 V, or 0 to 200 V
- input overvoltage protection

I had hoped that by presenting the basic 0 to 2 V interface first, more readers would attempt to build it due to its low cost. The extra capabilities presented this month can be added directly to the previously described hardware interface.

A Quick Review of the Interface Hardware

This DVM is designed around the Motorola MC14433 3 1/2 digit low power complimentary MOS analog to digital converter. The MC14433 is a modified dual ramp integrating analog to digital converter with multiplexed binary boded decimal (BCD) output. With the resistor values chosen it will perform approximately 25 conversions per second.

The full scale voltage value (ie: the value represented by the 3 1/2 digits after any input voltage division) is set by an MC1403 voltage reference integrated circuit. With 2.000 V applied to the V_{Ref} input of the MC14433, full scale is ±1.999 V. If 0.200 V is applied, full scale would be ±0.1999 V or ±199.9 mV.

The MC14433 can directly drive one LS TTL load. Since not all parallel input ports are LS TTL compatible, 74LS04s act as buffers and drivers on all digital voltmeter integrated circuit output pins. Data output is of course inverted and must be complemented before use.

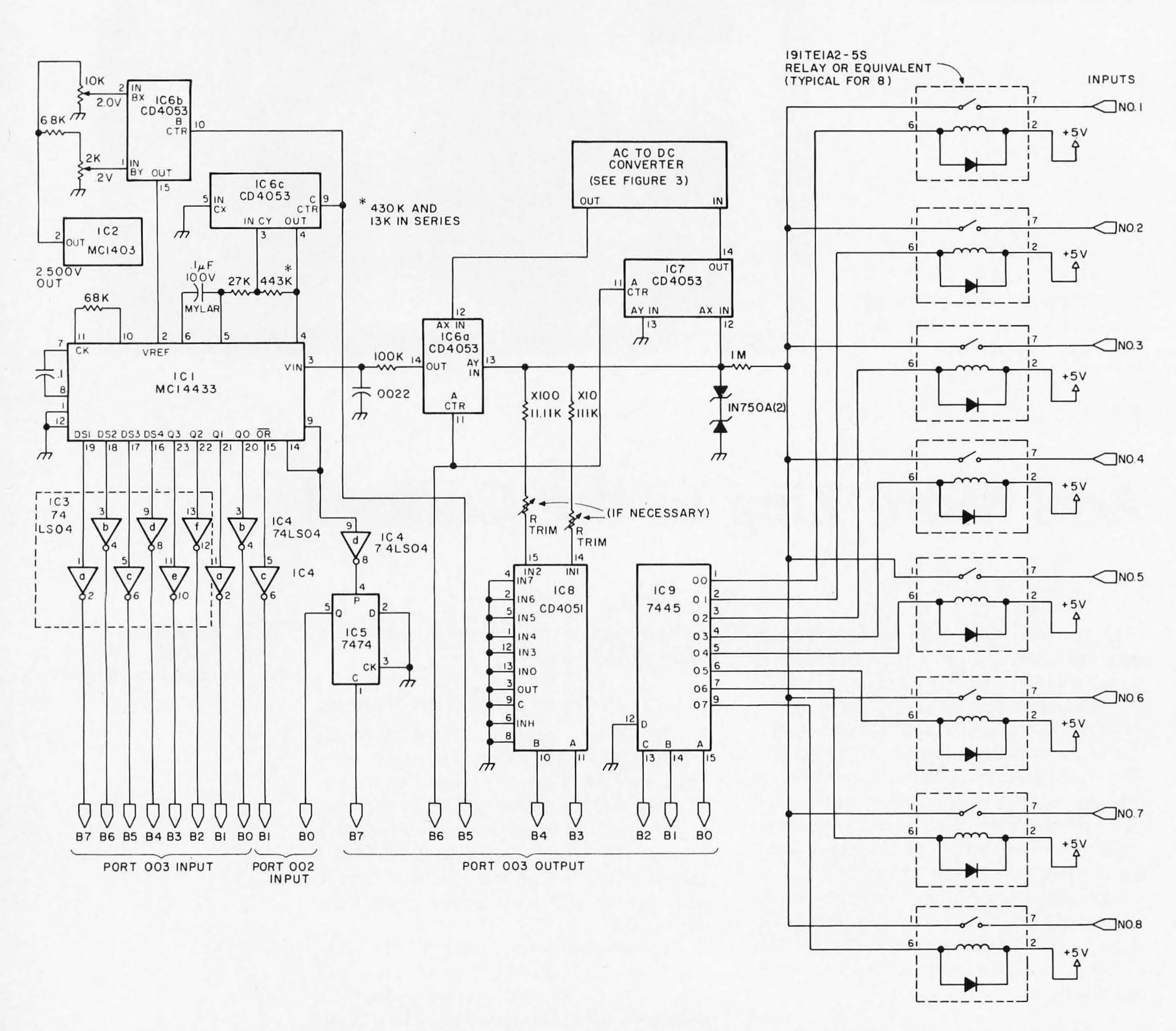


Figure 1a: The modified digital voltmeter, an expansion of last month's basic design. Changes include the addition of an input multiplexer, made up of eight dual in line package relays, and IC9, a 1 of 10 decoder. The modification allows the voltmeter to handle a wider variety of input voltages, both AC and DC. All resistors are 5% 1/4 W, and all capacitors are 100 V ceramic, unless otherwise indicated.

Number	Type	+5 V	GND	−5 V
IC1	MC14433	24	12	13
IC2	1403	1	3	
IC3	74LS04	14	7	
IC4	74LS04	14	7	
IC5	7474	14	7	
IC6	CD4053	16	8	7
IC7	CD4053	16	8	7
IC8	CD4051	16	8	7
IC9	7445	16	8	

Table 1: Power wiring table for figure 1.

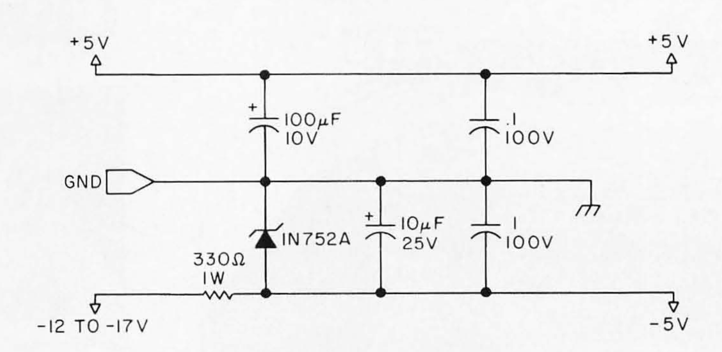


Figure 1b: A circuit enabling the experimenter to derive −5 VDC from an existing power supply having any output from −12 to −17 VDC. −5 VDC is needed to power the various CMOS switches used in this design (see figure 1c).

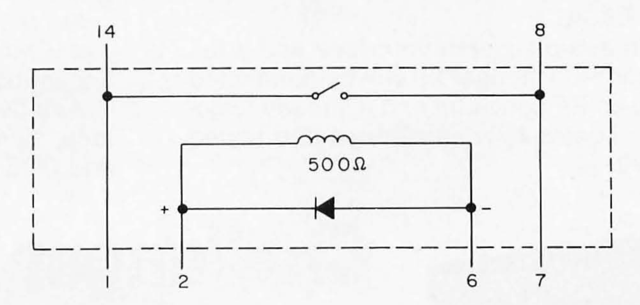


Figure 1c: Pin diagram of a Sigma relay, type 191TE1A2-5S 14 pin dual in line package.

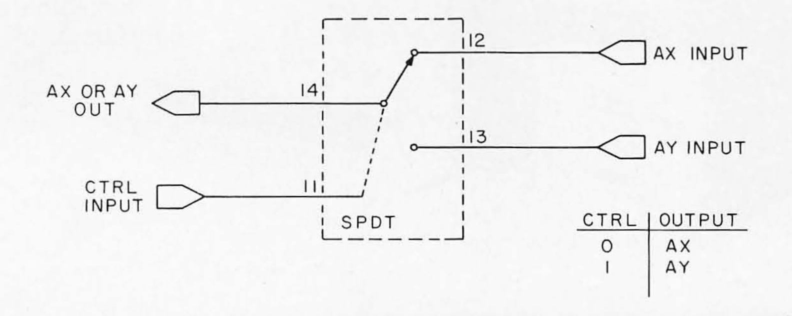


Figure 1d: Functional description of one switching section of a CD 4053 CMOS switch. The device acts like a remote controlled single pole double throw switch.

Continued on page 44

The data from the digital voltmeter to the computer is serial and parallel. There are four digit select lines and four binary coded decimal (BCD) data lines:

pin 23	Q_3	(Most significant bit)
pin 22	Q_2	
pin 21	Q_1	BCD, digit value outputs
pin 20	Q_0	
pin 19	DS1	(Most significant digit)
pin 18	DS2	
pin 17	DS3	Digit select outputs
pin 16	DS4	

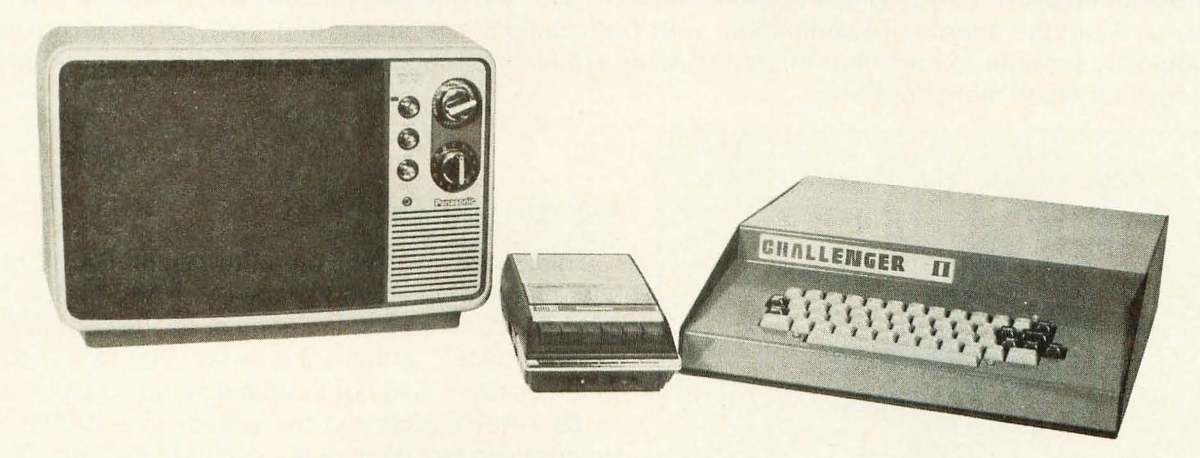
With respect to what the computer sees through the 74LS04 buffers, the digit select output is low when the respective digit is selected. The most significant digit (1/2 digit DS1) goes low immediately after an end of conversion pulse followed by the remaining digits sequencing from the most significant to the least significant digit. An interdigit blanking time of two clock periods is included internally to ensure that the BCD data has settled.

During the 1/2 digit (DS1), the polarity and certain status bits are available. Polarity is on Q_2 and a 1 will indicate negative. The 1/2 digit will appear on Q_3 and a 1 will indicate high.

Enhancements to the Basic DVM Interface

Photo 1 and figure 1 illustrate the fully modified DVM interface. It retains the basic interface structure outlined last month, but with some additional goodies. The interface is designed for attachment to decoded 8 bit parallel input and output ports and can be

Meet Challenger IIP from Ohio Scientific.



Unlike any other personal computer available today

Complete with BASIC in ROM and 4K RAM, Challenger IIP is the ideal computer for programs in BASIC.

BASIC is there the instant you turn the computer on with a full 32 x 64 character video display. Challenger IIP also comes with an Audio Cassette Interface for program storage. The user simply connects a Video Monitor or a TV via an RF Converter (not supplied) and the machine is ready to use.

Challenger IIP is ideal for both the home user who is new to computing or the experienced user who wants expansion capabilities. Challenger IIP comes with a four slot backplane and is expandable via the full Ohio Scientific product line, which includes 15 system boards offered in over 40 different versions.

Ohio Scientific has always maintained upward expandability from old models to new models, which is nice to know considering the rate at which technology is constantly improving. For example, Ohio Scientific's original 400 series products can be plugged right into the new Challenger IIP. And Ohio Scientific has 2 years of experience in building personal computers, so we're not new to this business unlike some of our competitors.

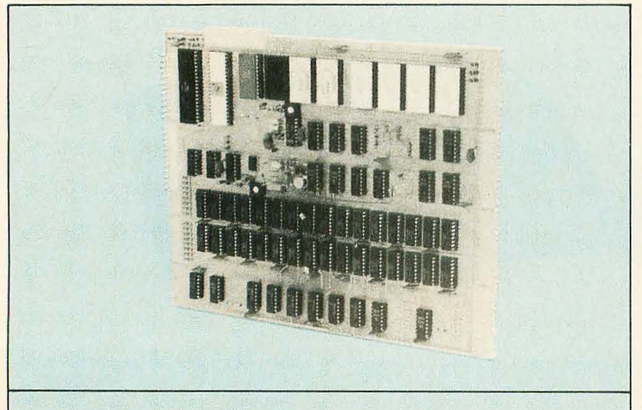
Complete with a full computer keyboard Challenger IIP comes fully assembled for $598 from Ohio Scientific.

Check the chart below and compare Challenger IIP with other BASIC in ROM computers. Unlike other personal computers, Challenger IIP has a much greater capacity for expansion and the capability to perform big computer functions with all of its big computer features.

	Ohio Scientific Challenger IIP	Other BASIC in ROM Computers
Processor	6502A	6502 or Z-80
Clock	1 or 2 MHz	slower
Display (Lines/Characters)	32/64	25/40 or 16/64
Keyboard	Full Computer (Capacitive Contact)	4 Function Calculator Type or Full Computer (Mechanical Contact)
Display Characters	256	128 or 64
Lower Case	Yes	No
Plotting	Yes	Yes
Audio Cassette Interface	Yes	Yes
BASIC	8K By Microsoft	some have only 4K BASIC
String Functions PEEK, POKE, User	Yes	Not Always
Machine Language Accessible	Yes	Not Always
Optional Assembler/Editor	Yes	No
Disk Option Available Now	Yes	No
In Case Memory Expansion Ability	36K	Less
Expansion Boards Available Now	15	None

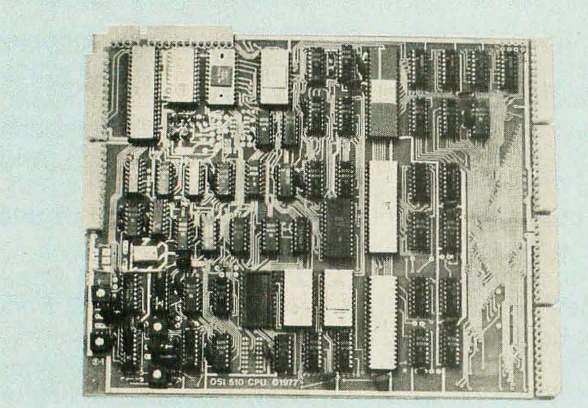
Introducing three boards only Ohio Scientific could build.

Ohio Scientific provides 15 system boards offered in over 40 different versions for Ohio Scientific Computer users. All of the boards are compatible with Ohio Scientific systems and many of them are by far technologically superior to any other microcomputer products on the market. And Ohio Scientific has the technology that made them possible.



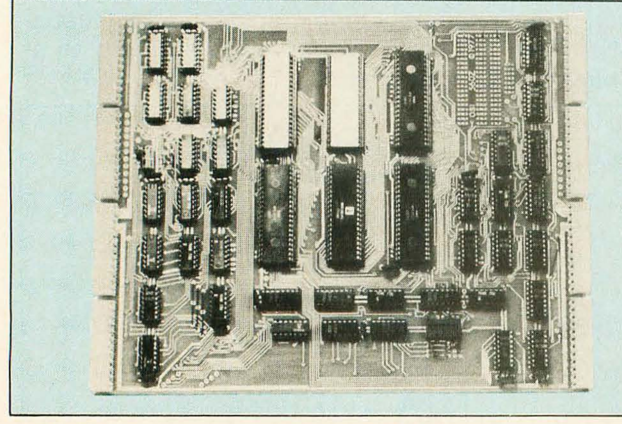
500 CPU Board

This board gives you our ultra-fast 8K BASIC in ROM with plenty of user workspace (4K RAM) for as little as $298.00. Use it as a standalone or as the CPU in a large system. BASIC is there the instant you turn it on. And in the October issue of *Kilobaud Magazine,* our version of 8K BASIC came out the winner in a BASIC timing comparison test of all of our competitors. The 500 is the fastest around!



510 Systems CPU Board

This is our unbelievable triple processor board! Complete with the 6502A, 6800, and Z-80 processors, this board allows you to run virtually all programs published for small computers. Available in the Challenger III, the 510 board is ideal for industrial development and research applications. There isn't another triple processor board like the 510 anywhere, except at Ohio Scientific!



560Z CPU Expander Board

The 560Z board is our multiprocessing board with a Z-80 and 6100 chip. This board allows you to run several processors simultaneously and the 6100 chip lets you run powerful PDP8 software with the 560Z. The 560Z board is the only multiprocessing board available for small computers, and Ohio Scientific makes it!

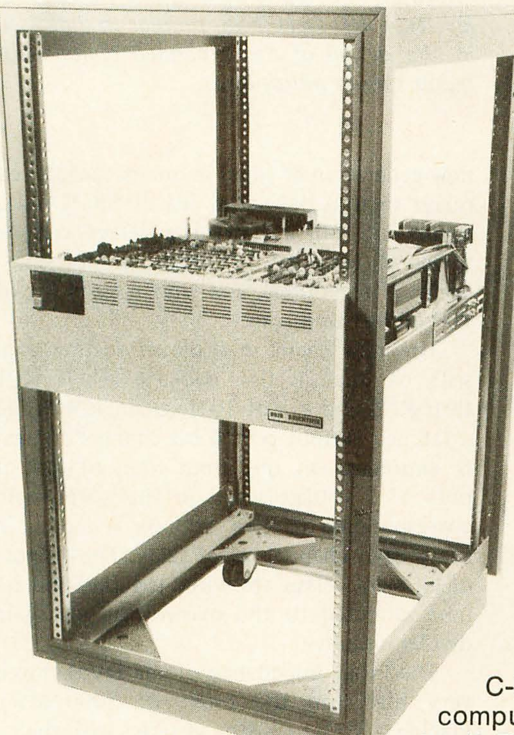
These three state-of-the-art CPUs are only a small part of the picture. Ohio Scientific's advanced technology offers you other unique features such as Multiport Memories, Distributed Processing, Big Disks with up to 300 megabytes on line, and Advanced Software.



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Continued from page 39

polled by a machine language subroutine. More on this later.

The following is a summary of the interface by port allocations. (Note: I have assigned particular octal port numbers to each byte. These designations will run directly with the software driver provided. If the reader wishes to assign some other port numbers, this is fine, but remember to modify the driver software to reflect the changes.)

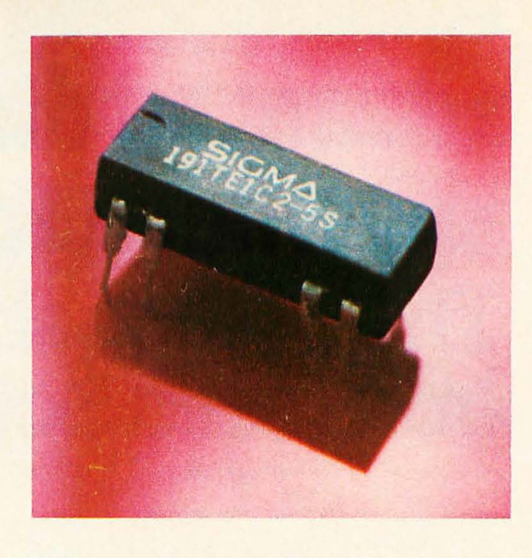


Photo 2: The Sigma dual in line package relay, type 191TE1C2-5S, similiar to that used in the design of the expanded digital voltmeter's input multiplexer.

Command Output Byte (Port 003 Out)

Bit	Function	Setting
B7	= EOC enable or disable	(Disable = 0 Enable = 1)
B6	= AC or DC select	(AC = 0; DC = 1)
B5	= 2.0 V or 0.2 V V_{Ref} select	(2.0 V = 0; 0.2 V = 1)
B4, B3	= Gain Code	see gain table
B2, B1, B0	= Channel select, 0 to 7	

B_4	B_3	Gain
0	0	×1
0	1	×10
0	0	×100
1	1	N/A (will result in ×1)

Status Input Byte (Port 002 In)

Bit	Function	
B7, B6, B5, B4, B3, B2	Not used	
B1	= Out of range	$-1.999\ V > V_{IN} > 1.999\ V$
B0	= End of conversion	$-199.9\ mV > V_{IN} > 199.9\ mV$

Data Input Byte (Port 003 In)

Bit	Function
B7	= 1st digit
B6	= 2nd digit
B5	= 3rd digit
B4	= 4th digit
B3, B2, B1, B0	BCD digit value

Most significant digit: when low true =

Bit	Function
B7	= 0
B6, B5, B4	N/A
B3	= 1/2 digit value
B2	= Polarity
B1	N/A
B0	= Ranging status bit

The most obvious change to the newly modified DVM board is the input multiplexer. Up to this point all the inputs were multiplexed through a CMOS CD4051 integrated circuit. This device performs quite satisfactorily for inputs in the range of 0 to 2 V. The maximum input voltage range it can handle is limited by its supply voltage (in this case ±5 V). Even if the supplies were increased to ±9 V (18 V absolute, which is the maximum supply for a CD4051B) a separate voltage divider would still be required at each input channel to keep the applied voltages within safe limits. To have a 0 to 200 V range selectable unit incorporating a CD4051 input maximum would require having eight separate programmable dividers and an overvoltage protection circuit on each channel in case the wrong divider values are chosen.

The preferred approach is to have only one divider network and one overvoltage circuit, but such an alternative requires that the input multiplexer be capable of handling all input voltage levels from 0 to 200 V! The answer is to use relays. Not the big 10 A clunkers you see in surplus catalogs, but the new generation of (dual in line package) reed relays such as the Series 191 by SIGMA (see photo 2). These particular relays can be driven directly by TTL logic, exhibit maximum 1 ms bounce, and have a rated life of 100 million operations.

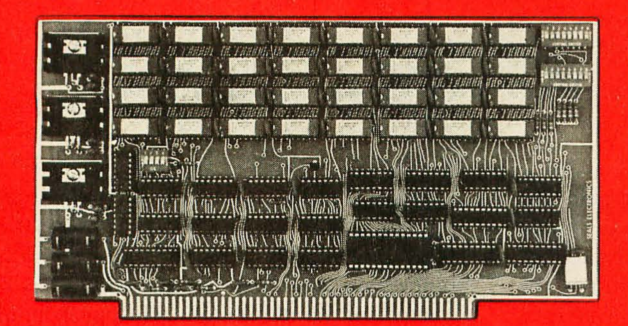
The new input multiplexer section consists of dual in line package relays RL1 thru RL8 and a 1 of 10 decoder, IC9. When a latched output port 3 bit channel address is impressed on the input lines of IC9, it puts a 0 voltage level on the output pin corresponding to that address and pulls in the proper channel select relay. The outputs of all eight relays are wired together and are next directed to the overvoltage and gain divider circuitry.

The input impedance of the DVM chip is very high (on the order of 1000 MΩ). Placing a 1 MΩ resistor in series with the relay outputs facilitates the addition of protection circuitry without compromising the interface's capabilities. This current limiting 1 MΩ resistor and two back-to-back zener diodes limit the absolute voltage seen by the MC14433 to about ±4 V (The MC14433's absolute limit is its power supply range, even though its usable input range is ±2 V.). If the correct gains are chosen and programmed to the interface, this protection should never be required. But, no one is perfect.

In addition to this function, the 1 MΩ resistor is one leg of a programmable divider network. Figure 2 shows the input subsystem in simplified terms. An AC to DC converter is also included and will be explained later. SW1 and SW2, parts of IC8, represent the gain selection section. The



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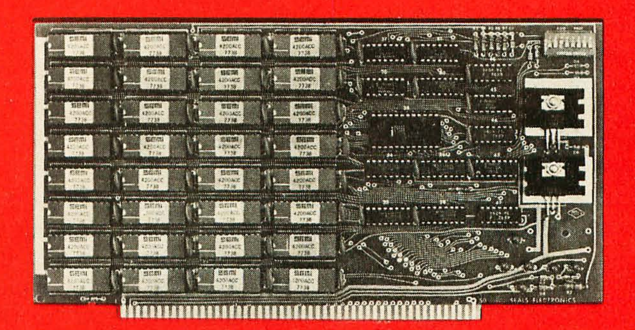


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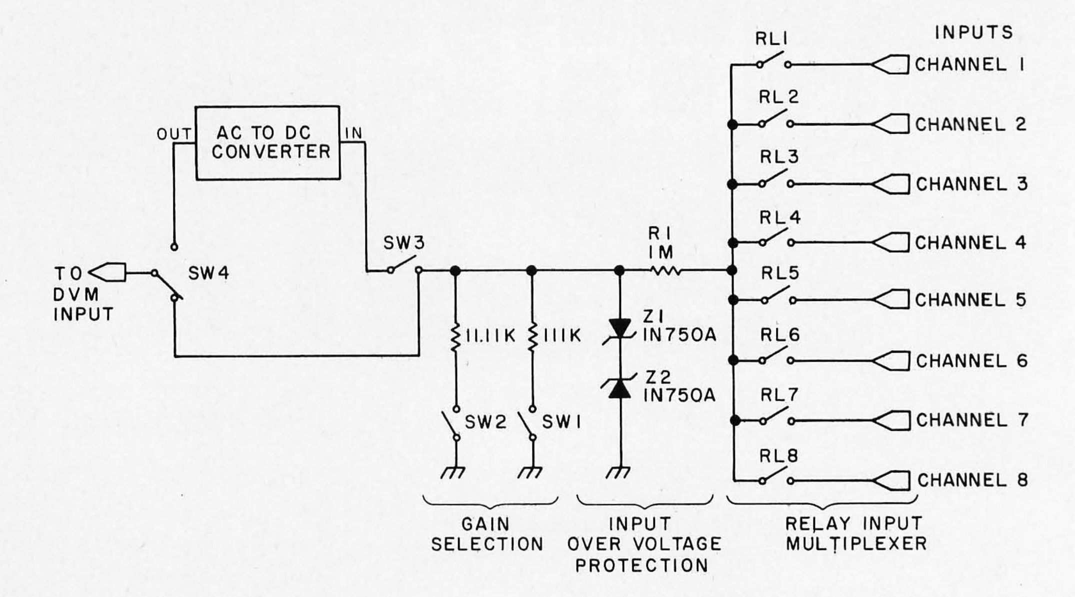


Figure 2: A simplified representation of the input section of the expanded digital voltmeter. The amount of gain and the AC to DC conversion option are selectable by means of CMOS switches.

switches are illustrated in a unit gain DC input mode. When an input relay is closed, its applied voltage is sent directly to the DVM integrated circuit input through the 1 MΩ resistor. The AC to DC converter is switched out of the system and with both SW1 and SW2 open, no dividers are in the circuit. If 1.400 V is applied through a closed relay, the DVM will read 1.400 V for that channel. If, on the other hand, 150 V is suddenly switched in on another relay with this SW1 and SW2 setting, the chips would be fried were it not for Z1 and Z2. At voltages of less than 4 absolute (±4 V) the diodes do nothing. When inputs exceed this absolute value, Z1 and Z2 clamp them to 4 V. The data acquired by the computer will indicate an out of range condition, since it is over 2 V, but at least it will not have evaporated.

How Do We Read 0 to 200 V Inputs?

Closing switch 2 forms a 10:1 divider network. If 8 V is applied and switch 1 is closed, the result is:

$$VA = \left(\frac{8}{R_1 + R_2}\right) \times R_2$$

$$= \left(\frac{8}{1.111\ M\Omega}\right) \times 111\ K$$

$$= 0.799\ V$$

$$\approx 0.800\ V$$

As you can see, the result of closing SW1 and applying the 111 K resistor is to divide the 8 V by 10 to get 0.799 V. Proper trimming of this 111 K resistor will give an output of 0.800 V. This value is compatible with the DVM integrated circuit input range, and when read by the computer, will be equal to 0.800 V. The programmer should keep in mind that a divider is used on this channel and should multiply the result by 10 to obtain 8.00 V.

Closing switch 2 forms a 100:1 divider. The mathematics is the same except that the divider resistor is 11.11 K instead of 111 K. An 8 V input appears at the DVM input as 0.080 V, while 150 V becomes 1.500 V.

AC to DC Converter

An additional bonus of this interface is AC to DC conversion on any input channel. Figure 3 shows the schematic of the AC to DC converter section of the interface. Bit 6 of output port 003 controls the application of this function. When it is high, SW3 and SW4 are in the positions shown in figure 2. In this state the AC to DC converter is switched out of the circuit and the DVM gets its input directly from the divider section. When bit 6 is programmed to be a low level, switches 3 and 4 switch to their alternate positions and route the input signal from the divider network through the AC to DC converter. The resulting signal is equal to the average RMS value of the applied input signal. This is basically the same type of circuit as the kind included in many single channel digital meters.

The AC to DC converter consists of three sections of an LM324, IC10. IC10A is a high impedance input buffer with variable offset adjustment. When the converter is switched into play, it must have a high input im-

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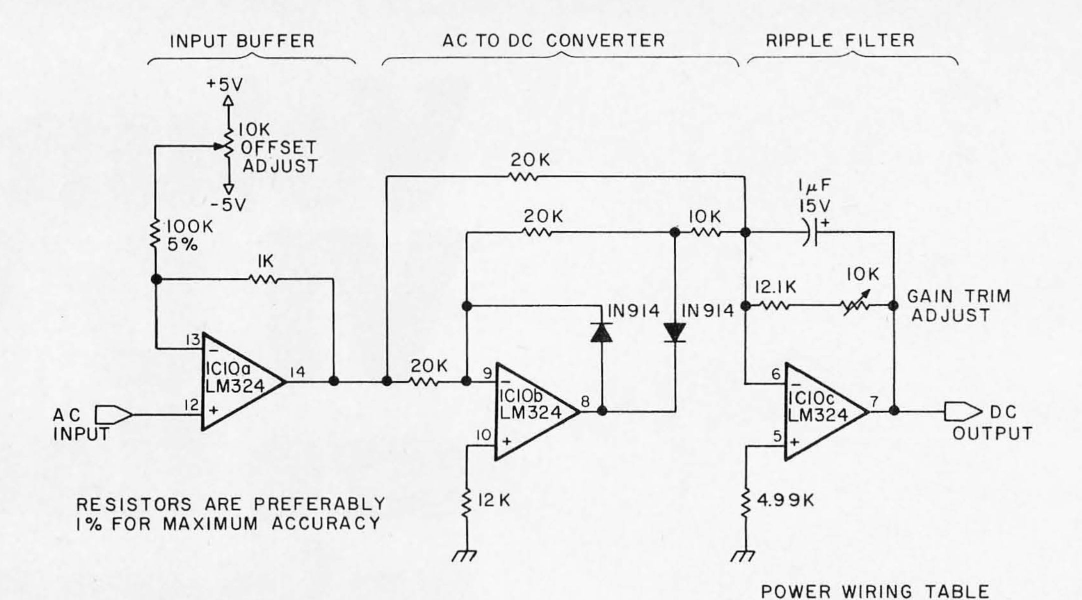


Figure 3: Circuitry of the AC to DC converter used by the digital voltmeter. All resistors are 1% except where shown.

POWER WIRING TABLE

NUMBER	TYPE	+5V	-5V
IC10	LM324	4	11

pedance to avoid loading down the divider network. IC10B is the actual AC to DC conversion section. Its output is a current proportional to the AC input voltage. IC10C converts this current to a voltage and provides ripple filtering. One consideration to keep in mind is that, since this is a multiplexing analog to digital converter, the usual DC blocking capacitor at the input of the AC to DC converter has been removed. Given the particular circuit impedances and desired frequency range the converter should cover, the input capacitor had to be removed because it couldn't respond quickly enough. The result is an AC to DC converter that will pass both AC and DC signals; only the AC converted signals should be used, however.

When a 1.0 V peak AC signal (60 Hz) is applied to the converter, the output should be +0.707 VDC. If by accident the AC converter is switched into a DC signal, the output of the converter will be 1.414 times the true DC input. Keep a close watch on your program command byte to the interface.

Adding a 199.9 mV Range

Up to this point we have discussed additions to the basic circuit that allow range selections of 0 to 2 V, 0 to 20 V, and 0 to 200 V. Circuit changes can be incorporated to extend the DVM range in the opposite direction. Figure 4 illustrates the voltage reference and range selection setup of this interface. The MC14433 can also be configured to cover a range of 0 to ±199.9 mV. When bit 5 of port 003 is low, switches 5 and 6 are in the positions shown. A ratiometric converter has a range determined by the applied V_{Ref}, which would be 2.000 V in this instance. With SW5 open, the integrating time constant is set by using a 470 K resistor (formed by the series combination of 443 K and 27 K). With bit 5 set to a 1, the converter changes its V_{Ref} level to 0.200 V and its integration resistor to 27 K. These changes are the only ones necessary for 0 to 0.2 V range selection.

A Less Complicated Driver

The driver was explained last month in detail. It was designed to be as fast as possible. The relay multiplexer added this month unfortunately cannot operate at that speed without modification. I have included a new driver subroutine written especially for this application (see listing 1).

The interface driver is a relocatable subroutine which is polled by a call instruction. The driver is written for page 140 (octal) but is easily relocatable. It occupies less than one 256 byte page of memory and is written for the Z-80 processor. It is especially designed

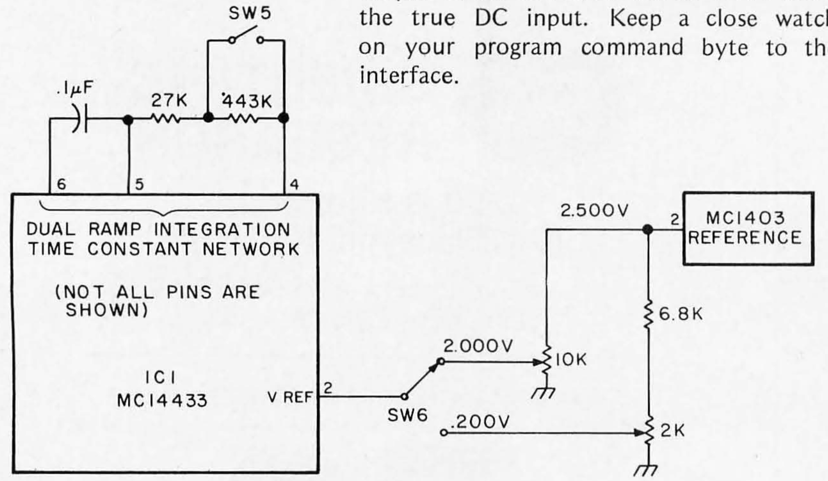


Figure 4: A simplified detail of figure 1, showing the V_{ref} and integration time constant circuitry.

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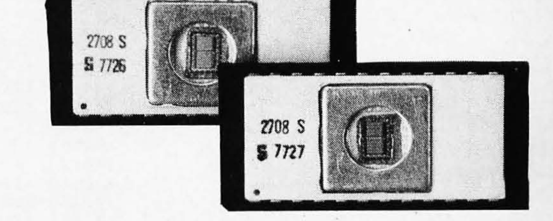
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Listing 1: An assembly language program for driving the MC14433 3 1/2 digit analog to digital converter, written for the Z-80.

```
140000                     0140 DIP     EQU  3       DATA INPUT PORT NUMBER
140000                     0150 SIP     EQU  2       STATUS INPUT PORT NUMBER
140000                     0160 COP     EQU  3       COMMAND OUTPUT PORT NUMBER
140000                     0170 EEOC    EQU  200     ENABLE EOC INPUT
140000                     0180 DEOC    EQU  000     DISABLE EOC INPUT
140000                     0190 *
140000                     0200 *
140000                     0210 * CONVERTED CHANNEL DATA BUFFERS
140000                     0220 *
140000 000 000             0230 CHAN0   DW   000000
140002 000 000             0240         DW   000000
140004 000 000             0250 CHAN1   DW   000000
140006 000 000             0260         DW   000000
140010 000 000             0270 CHAN2   DW   000000
140012 000 000             0280         DW   000000
140014 000 000             0290 CHAN3   DW   000000
140016 000 000             0300         DW   000000
140020 000 000             0310 CHAN4   DW   000000
140022 000 000             0320         DW   000000
140024 000 000             0330 CHAN5   DW   000000
140026 000 000             0340         DW   000000
140030 000 000             0350 CHAN6   DW   000000
140032 000 000             0360         DW   000000
140034 000 000             0370 CHAN7   DW   000000
140036 000 000             0380         DW   000000
140040                     0390 *
140040                     0400 * INTERMEDIATE DATA BUFFERS
140040                     0410 *
140040 000                 0430 CHAN    DB   000     CURRENT CHANNEL NUMBER
140041 000 000             0440 CCP     DW   000000 COMMAND CHANNEL PARAMETER
140043                     0460 *
140043                     0470 *
140043                     0480 *** START A/D CONVERTER
140043                     0490 *
140043                     0550 *
140043 173                 0560 START   LD   A,E
140044 062 041 140         0570         LD   (CCP),A
140047 346 007             0580         AND  007
140051 062 040 140         0590         LD   (CHAN),A
140054 335 041 000 140     0600         LD   IX,CHAN0
140060 026 000             0910         LD   D,0
140062 137                 0920         LD   E,A
140063 313 043             0930         SLA  E       CALCULATE BUFFER OFFSET
140065 313 043             0940         SLA  E
140067 335 031             0950         ADD  IX,DE
140071                     0960 *
140071                     0970 * SELECT CHANNEL AND START CONVERSION
140071                     0980 *
140071 006 003             0985         LD   B,3     SET CYCLE COUNT
140073 072 041 140         0990 SCSC    LD   A,(CCP)
140076 323 003             1000         OUT  COP     SELECT CHANNEL
140100 315 243 140         1005         CALL DELAY
140103 366 200             1010         OR   EEOC    ENABLE EOC OUTPUT
140105 323 003             1020         OUT  COP     COMMAND A/D CONVERTER
140107                     1030 *
140107                     1040 * WAIT FOR EOC
140107                     1050 *
140107 333 002             1060 WEOC    IN   SIP     READ CONVERTER STATUS
140111 313 107             1070         BIT  0,A     TEST FOR EOC
140113 050 372             1080         JR   Z,WEOC JUMP IF NOT READY
140115 020 354             1085         DJNZ  SCSC
140117 313 117             1090         BIT  1,A     TEST FOR OVERANGE
140121 040 066             1100         JR   NZ,OVER JUMP IF TRUE
140123                     1110 *
140123                     1120 * CONVERSION DONE;PROCESS FIRST (MSD) DIGIT
140123                     1130 *
140123 006 200             1140 MSD0    LD   B,200   SELECT DIGIT 1
140125 315 232 140         1150         CALL RDIG    WAIT AND READ DIGIT 1
140130 057                 1160         CPL
140131 017                 1170         RRCA RIGHT  JUSTIFY DIGIT VALUE
140132 017                 1180         RRCA
140133 017                 1190         RRCA
140134 346 001             1200         AND  1       ISOLATE
140136 036 000             1210         LD   E,0     INITIALIZE STATUS BYTE
140140 313 122             1220         BIT  2,D     TEST POLARITY
140142 040 002             1230         JR   NZ,MSD3 JUMP IF POSITIVE
140144 036 200             1240         LD   E,200   LOAD POLARITY SIGN
140146                     1440 *
140146                     1450 * SAVE MSD AND CURRENT POLARITY
140146                     1460 *
140146 263                 1470 MSD3    OR   E       ADD POLARITY SIGN TO MSD
140147 335 167 000         1480         LD   (IX+0),A SAVE IN DATA BUFFER
140152                     1500 *
140152                     1510 * PROCESS 2ND DIGIT
140152                     1520 *
140152 313 010             1530         RRC  B       SELECT DIGIT 2
140154 315 232 140         1540         CALL RDIG    WAIT AND READ DIGIT
140157 346 017             1550         AND  017     ISOLATE
140161 335 167 001         1560         LD   (IX+1),A STORE SECOND DIGIT
140164                     1570 *
140164                     1580 * PROCESS 3RD DIGIT
140164                     1590 *
140164 313 010             1600         RRC  B       SELECT 3RD DIGIT
140166 315 232 140         1610         CALL RDIG    WAIT AND READ DIGIT
140171 346 017             1620         AND  017     ISOLATE
140173 335 167 002         1630         LD   (IX+2),A STORE
140176                     1640 *
```

Listing 1, continued:

```
140176                   * PROCESS 4TH DIGIT
140176                   *
140176 313 010                  RRC  B        SELECT 4TH DIGIT
140200 315 232 140              CALL RDIG     WAIT AND READ DIGIT
140203 346 017                  AND  017      ISOLATE
140205 335 167 003              LD   (IX+3),A STORE
140210 311               RAPUP  RET
140211                   *
140211                   * LOAD 2.000 OVERRANGE VALUE INTO DATA BUFFER
140211                   *
140211 076 002           OVER   LD   A,2      LOAD MSD VALUE
140213 335 167 000              LD   (IX+0),A
140216 257                      XOR  A
140217 335 167 001              LD   (IX+1),A LOAD LSD VALUES
140222 335 167 002              LD   (IX+2),A
140225 335 167 003              LD   (IX+3),A
140230 030 356                  JR   RAPUP
140232                   *
140232                   *
140232                   * READ DIGIT ROUTINE
140232                   *
140232 333 003           RDIG   IN   DIP      READ DATA BYTE
140234 057                      CPL           CONVERT TO HIGH TRUE LOGIC
140235 127                      LD   D,A      SAVE COPY
140236 240                      AND  B        TEST FOR GIVEN DIGIT READY
140237 050 371                  JR   Z,RDIG   JUMP IF NOT
140241 172                      LD   A,D      RESTORE A REGISTER
140242 311                      RET           RETURN TO CALLER
140243 016 377           DELAY  LD   C,377
140245 015               DEL1   DEC  C
140246 310                      RET  Z
140247 030 374                  JR   DEL1
```

to run with an Extended BASIC which has instructions to access memory and IO ports, and can call a machine language program.

The driver is exercised by a call instruction. In Digital Group Maxi BASIC, the call instruction looks like this: LET X=CALL (24611,64). The BASIC interpreter goes to decimal location 24611 to execute the call and decimal 64 is put in the DE register pair. To the driver, this call is a signal to perform an analog to digital conversion. The contents of the DE register tell it which channel to convert, whether it should be AC or DC, and which V_{Ref} and gain to use. One channel is converted every time the driver is called. The information sent in the DE register at the time of the call is the command output byte (port 003), and each bit has the designations previously listed. The only difference is that bit 7 (the enable disable bit to the analog to digital converter) is sent out as a 0 when doing a call. The driver will set it to an enable condition after it has pulled in the proper relay and allowed a 1.3 ms bounce delay.

When the driver concludes its operation, it has acquired a 3 1/2 digit voltage reading from the DVM which is represented by four bytes. These four bytes are placed in a table in memory. The eight channels of data constitute a 32 byte table. The location of a particular channel's data can be found by a simple expression:

4 byte data location starts at $L + [4(N-1)]$

where L = starting address of table
N = channel number (1 to 8)

Listing 2: A supervisory program for controlling the expanded digital voltmeter written in extended BASIC.

```
120 REM 8 CHANNEL 3 1/2 DIGIT AC/DC PROGRAMABLE RANGE DVM -S.CIARCIA
130 REM REV. 1.9
140 REM BOARD CHECK OUT PROGRAM
150 REM
160 REM
170 LET M1=24576
180 REM THIS IS PAGE 140(OCTAL)
190 LET M2=24611
200 REM THIS IS THE CALL ADDRESS
210 REM
220 PRINT
230 PRINT
240 PRINT"DO YOU WANT TO SCAN PREVIOUSLY CHOSEN CHANNELS OR"
250 PRINT"SELECT NEW ONES ?   SCAN OR SELECT OR STOP"
260 INPUT S$
265 IF S$="STOP" THEN GOTO 2000
270 IF S$="SCAN" THEN GOTO 830
280 PRINT"SELECT ALL VALUES OR CHANGE ONE CHANNEL"
290 PRINT"ALL OR ONE"; :INPUT S$
300 IF S$<>"ONE" THEN GOTO 420
310 PRINT
320 PRINT"WHICH CHANNEL DO YOU WISH TO CHANGE "; :INPUT C
330 PRINT"PRESENTLY CHOSEN VALUES ARE "
340 IF D(C)=1 THEN R1=.2 ELSE R1=2.0
350 PRINT"VREF.=";R1;" VOLTS   DIVIDER GAIN IS X";F(C);"   CONDITIONING IS FOR ";
360 IF C(C)=1 THEN PRINT"DC" ELSE PRINT"AC"
370 LET A(C)= 1 :GOSUB 590
380 GOSUB 750
390 PRINT"ANOTHER CHANNEL TO CHANGE ?  Y OR N"; :INPUT R$
400 IF R$<>"N" THEN GOTO 320
410 GOTO 830
420 PRINT
425 PRINT"INPUT CHANNEL PARAMETERS"
430 PRINT"GAIN MULTIPLIER IS  1,10 OR,100"
440 PRINT"ENTER CHANNEL PARAMETERS AS REQUIRED"
450 PRINT :PRINT: PRINT
460 FOR C=1 TO 8
470 PRINT"DO YOU WANT TO READ CHANNEL ";C;"        Y OR N OR EXIT";
480 INPUT A$
490 IF A$="EXIT" THEN GOTO 240
500 LET A(C)=0
510 IF A$="N" THEN GOTO 710
520 IF A$="Y" THEN LET A(C)=1
530 IF A$<>"Y" THEN GOTO 470
540 GOSUB 590
550 GOTO 700
560 REM
570 REM
580 REM THIS IS THE PARAMETER SETTING SUBROUTINE
590 PRINT"GAIN ",
600 INPUT B(C)
610 LET F(C)=B(C)
620 LET E(C)=0
630 IF B(C)=10 THEN LET E(C)=8 :GOTO 650
640 IF B(C)=100 THEN LET E(C)=16 :GOTO 650
650 PRINT"ENTER 1 FOR DC OR 0 FOR AC",
660 INPUT C(C)
670 PRINT"ENTER 1 FOR .2 VOLT, OR 0 FOR 2.0 VOLT DVM VREF.";
680 INPUT D(C)
690 RETURN
700 PRINT
710 NEXT C
720 REM X1 TO X8 ARE THE CALL SETPOINTS
730 GOSUB 750
740 GOTO 810
750 FOR J=1 TO 8
760 LET X(J)=64*C(J)+32*D(J)+E(J)+J-1
770 REM X(J) IS LOADED WITH THE BIT PATTERN WHICH IS
780 REM PUT IN THE DE REG. PAIR DURING THE CALL INSTRUCTION
790 NEXT J
800 RETURN
810 PRINT
820 PRINT
830 REM THIS ROUTINE DETERMINES WHICH CHANNELS ARE TO BE CONVERTED"
840 FOR C=1 TO 8
850 IF A(C)=0 THEN GOTO 870
860 LET H=CALL(M2,X(C))
870 NEXT C
880 REM THIS ROUTINE PRINTS THE VALUES IN THE MEMORY TABLE
890 LET Z=A(1)+A(2)+A(3)+A(4)+A(5)+A(6)+A(7)+A(8)
900 IF Z=0 THEN PRINT"NO CHANNEL PARAMETERS HAVE BEEN CHOSEN" :GOTO 450
910 LET D=M1
920 FOR L=1 TO 8
930 GOSUB 1030
940 IF A(L)=0 THEN 990
950 IF D(L)=0 THEN GOTO 970
960 IF Y1>=.2 THEN PRINT"CHANNEL ";L;" IS OUT OF RANGE" : GOTO 990
```

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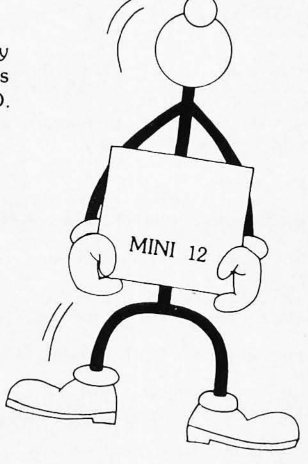
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Circle 109 on inquiry card.

Listing 2, continued:

```
970 IF Y1>=2 THEN PRINT"CHANNEL ";L;" IS OUT OF RANGE" :GOTO 990
980 GOSUB 1230
990 NEXT L
1000 GOTO 170
1010 REM
1020 REM
1030 REM THIS ROUTINE EXAMINES THE MEMORY TABLE
1040 REM AND CONVERTS THE 4 BYTES TO A 3 1/2 DIGIT VOLTAGE
1050 LET Q1=EXAM(D)
1060 LET Q=Q1
1070 IF Q1>=128 THEN LET Q=Q1-128
1080 D=D+1
1090 LET W=EXAM(D)
1100 D=D+1
1110 LET E=EXAM(D)
1120 D=D+1
1130 LET R=EXAM(D)
1140 LET D=D+1
1150 LET Y=Q+(.1*W)+(.01*E)+(.001*R)
1160 LET Y1=Y
1170 LET Y=B(L)*Y
1180 IF D(L)=1 THEN LET Y1=Y/10
1190 RETURN
1200 REM
1210 REM
1220 REM
1230 REM THIS SUBROUTINE PRINTS OUT THE VOLTAGE VALUES
1240 PRINT"CHANNEL ";L;" IS ";
1250 IF Q1<128 THEN PRINT" "; : GOTO 1270
1260 IF Q1>=128 THEN PRINT"-";
1270 IF D(L)=1 THEN PRINT %7F4;Y1;" VOLTS "; :GOTO 1310
1280 IF B(L)=100 THEN PRINT %5F1;Y;" VOLTS ";
1290 IF B(L)=10 THEN PRINT %5F2;Y;" VOLTS ";
1300 IF B(L)=1 THEN PRINT %6F3;Y;" VOLTS ";
1310 IF C(L)=0 THEN PRINT"AC";
1320 PRINT
1330 RETURN
2000 END
READY
```

Listing 3: A sample of the program in listing 2 being used to read five different inputs.

```
DO YOU WANT TO SCAN PREVIOUSLY CHOSEN CHANNELS OR
SELECT NEW ONES ?   SCAN OR SELECT OR STOP
?SELECT
SELECT ALL VALUES OR CHANGE ONE CHANNEL
ALL OR ONE?ALL

INPUT CHANNEL PARAMETERS
GAIN MULTIPLIER IS  1,10 OR,100
ENTER CHANNEL PARAMETERS AS REQUIRED

DO YOU WANT TO READ CHANNEL  1          Y OR N OR EXIT?Y
GAIN      ?1
ENTER 1 FOR DC OR 0 FOR AC      ?1
ENTER 1 FOR .2 VOLT, OR 0 FOR 2.0 VOLT DVM VREF.?0

DO YOU WANT TO READ CHANNEL  2          Y OR N OR EXIT?Y
GAIN      ?1
ENTER 1 FOR DC OR 0 FOR AC      ?1
ENTER 1 FOR .2 VOLT, OR 0 FOR 2.0 VOLT DVM VREF.?0

DO YOU WANT TO READ CHANNEL  3          Y OR N OR EXIT?N
DO YOU WANT TO READ CHANNEL  4          Y OR N OR EXIT?N
DO YOU WANT TO READ CHANNEL  5          Y OR N OR EXIT?N
DO YOU WANT TO READ CHANNEL  6          Y OR N OR EXIT?Y
GAIN      ?10
ENTER 1 FOR DC OR 0 FOR AC      ?1
ENTER 1 FOR .2 VOLT, OR 0 FOR 2.0 VOLT DVM VREF.?0

DO YOU WANT TO READ CHANNEL  7          Y OR N OR EXIT?Y
GAIN      ?10
ENTER 1 FOR DC OR 0 FOR AC      ?0
ENTER 1 FOR .2 VOLT, OR 0 FOR 2.0 VOLT DVM VREF.?0

DO YOU WANT TO READ CHANNEL  8          Y OR N OR EXIT?Y
GAIN      ?100
ENTER 1 FOR DC OR 0 FOR AC      ?1
ENTER 1 FOR .2 VOLT, OR 0 FOR 2.0 VOLT DVM VREF.?0


CHANNEL  1 IS .  1.515 VOLTS
CHANNEL  2 IS     .114 VOLTS
CHANNEL  6 IS - 9.48 VOLTS
CHANNEL  7 IS   9.40 VOLTS AC
CHANNEL  8 IS  118.2 VOLTS
```

To use the converter with BASIC, the program merely calls for a particular channel conversion and then extracts the appropriate data from the table. Listing 2 is a BASIC program which details the entire procedure.

CAUTION:

One caution should be kept in mind when using this interface to measure AC signals: the ground on the interface board is the same ground as the computer. If you use the interface board to read 115 VAC line voltage, a potential short circuit exists unless either the computer or the measured voltage is isolated. Since isolating the computer equipment would constitute a violation of many electrical codes, only isolated AC signals should be read. A common measurement case which meets this criterion is the AC secondary section of a low voltage power supply such as the unit which runs your computer.

Conclusion

I often see construction projects which are beyond the means of some experimenters. With these two articles I've attempted to reverse the trend by giving the complete design of a low cost DVM interface. By adding more components, such as relays, this interface can become a full fledged data acquisition system.

I'm sure by now, after seeing designs from me for a serial IO interface, parallel IO, digital to analog converter, and now an analog to digital converter, most readers will realize that I'm constructing a complete computer front end for measurement and control applications in the home and lab. We still need 115 VAC IO interfacing, a real time and time of day clock, and a few other items. When we're finished we'll investigate closed loop control and interrupt drivers.

I am always interested in readers' comments on the ideas for applications. I work interactively, so don't hesitate to write me (and include a self-addressed stamped envelope for replies).

Next month: a memory jump detector!■

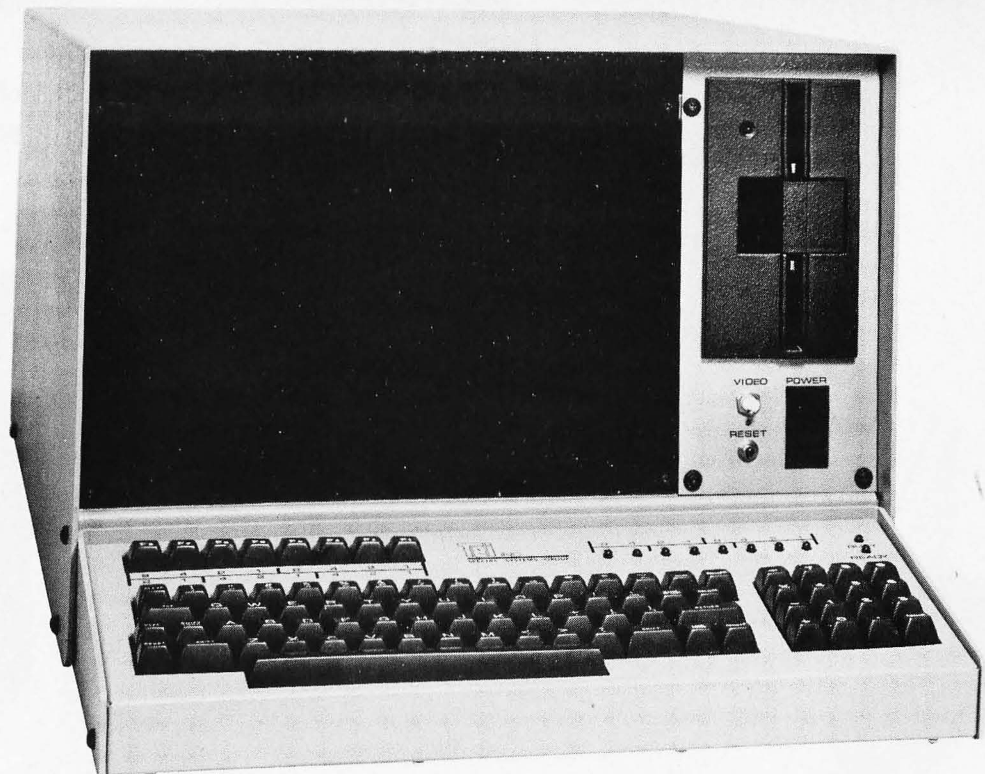
The following interface components are available postpaid in the continental US from:

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Kit 1: ICs 1, 2, 3, 4, 5 and 8 to build the 0 to 2 V 8 channel unit described in the first part of this 2 part series presented last month. $29.95

Kit 2: Printed circuit board with 44 pin edge connector which supports the circuitry for this month's expanded DVM interface as well as the basic unit and the components of kit 1. $64.95.

Kit 3: Assembled and tested unit consisting of kits 1 and 2. $79.95



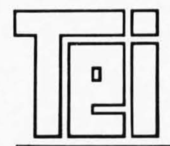
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A Floppy Disk Interface

David M Allen
Electronics Consultant
1317 Central Av
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Once it would have been appropriate to begin this article with a paragraph justifying the use of a floppy disk in a hobbyist system. Today that paragraph is unnecessary for two reasons: First, most of the more ambitious microprocessor users have already convinced themselves of the need for fast programmable memory; second, a growing number of users have begun to discover that the hardware required to interface a floppy disk to a microprocessor doesn't need to be very complex, and certainly not as expensive as some of the purveyors of professional equipment would have us believe. This article presents a straightforward way to control a floppy disk drive with a microprocessor.

While definitely not a project for a beginner, the interface itself is relatively simple and well within the grasp of anyone who has built other computer equipment. It is conceivable that people without an oscilloscope might be able to build the interface blindly and get it working successfully, but I strongly discourage them from doing so. A good oscilloscope, particularly one with dual trace and variable delay features, is highly recommended for testing the interface and drive during construction. Once built and working, the unit should not need any adjustments.

I do not attempt to provide all of the cookbook information necessary to thoroughly educate the novice in the ways of floppy disks. Rather, I provide an overview of one system, cover all the basic features and functions, and draw examples from a working system. I hope to encourage people to build their own systems as an alternative to buying someone else's.

This interface is intended for hardware sectored disks and disk drives, although the basic technique could be extended by the use of more on board buffer memory to permit the use of a software sectored format. This interface is specifically designed for the Memorex 651 drive, but the use of an on board buffer makes the interface independent of the associated processor's speed, and allows it to be used with virtually any processor. At least one person has used a similar interface with a 4004 for three years. The use of an on board buffer did not add to the chip count of the interface; if anything, it reduced it. The chip count is 31, and all chips are small or medium scale integration TTL with the exception of the buffer memory.

Table 1: Power wiring table for the integrated circuits used in figure 1.

Number	Type	+5 V	GND
IC1	7400	14	7
IC2	74175	16	8
IC3	7400	14	7
IC4	2102A6	10	9
IC5	74177	14	7
IC6	74125	14	7
IC7	74125	14	7
IC8	7404	14	7
IC9	7416	14	7
IC10	7416	14	7
IC11	7404	14	7
IC12	7404	14	7
IC13	7408	14	7
IC14	2102A6	10	9
IC15	74177	14	7
IC16	74125	14	7
IC17	7430	14	7
IC18	7411	14	7
IC19	7410	14	7
IC20	74175	16	8
IC21	74177	14	7
IC22	74121	14	7
IC23	74177	14	7
IC24	2102A6	10	9
IC25	74177	14	7
IC26	74177	14	7
IC27	7474	14	7
IC28	7420	14	7
IC29	7430	14	7
IC30	7474	14	7
IC31	7474	14	7
IC32	7404	14	7

Circuit Description

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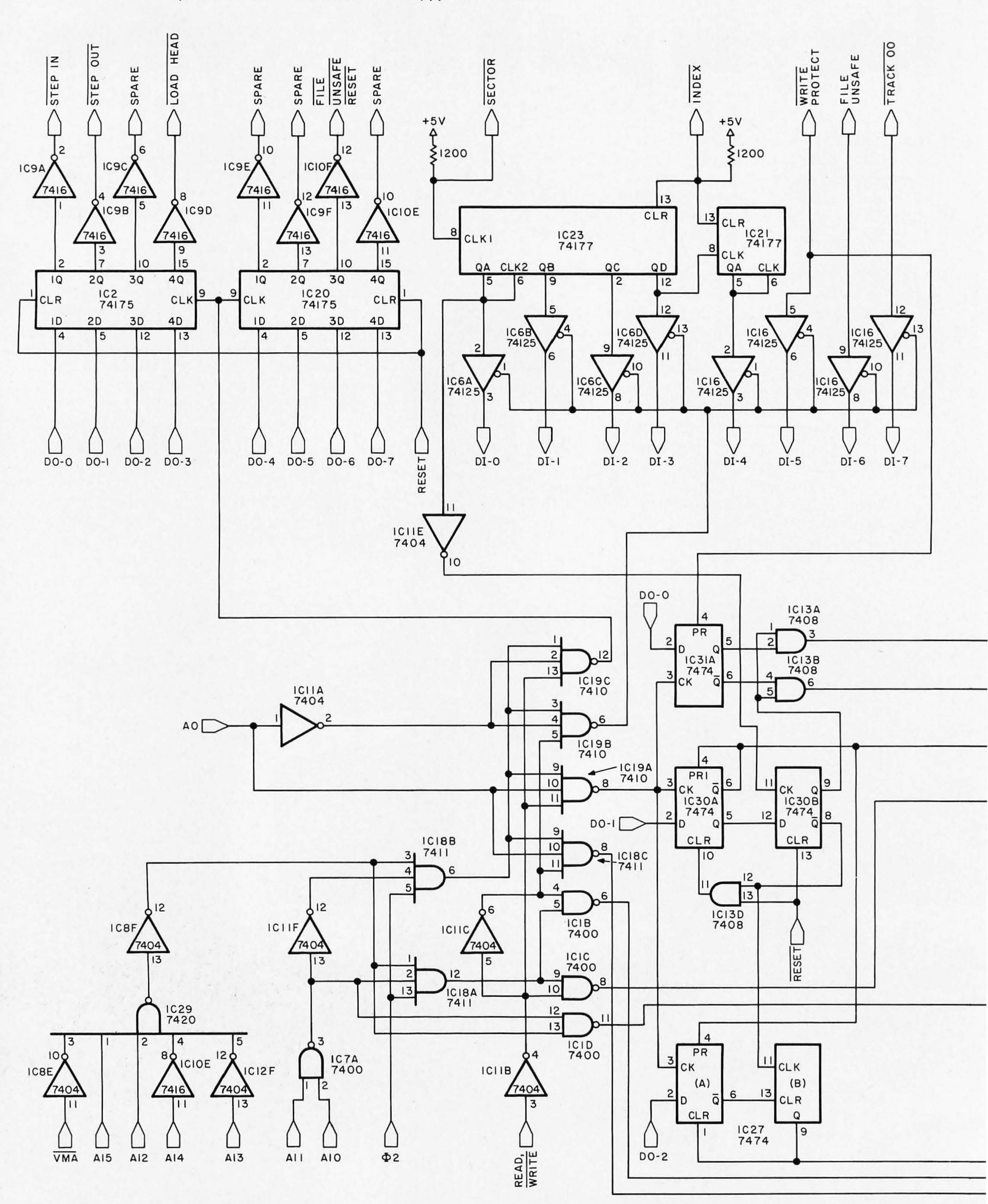
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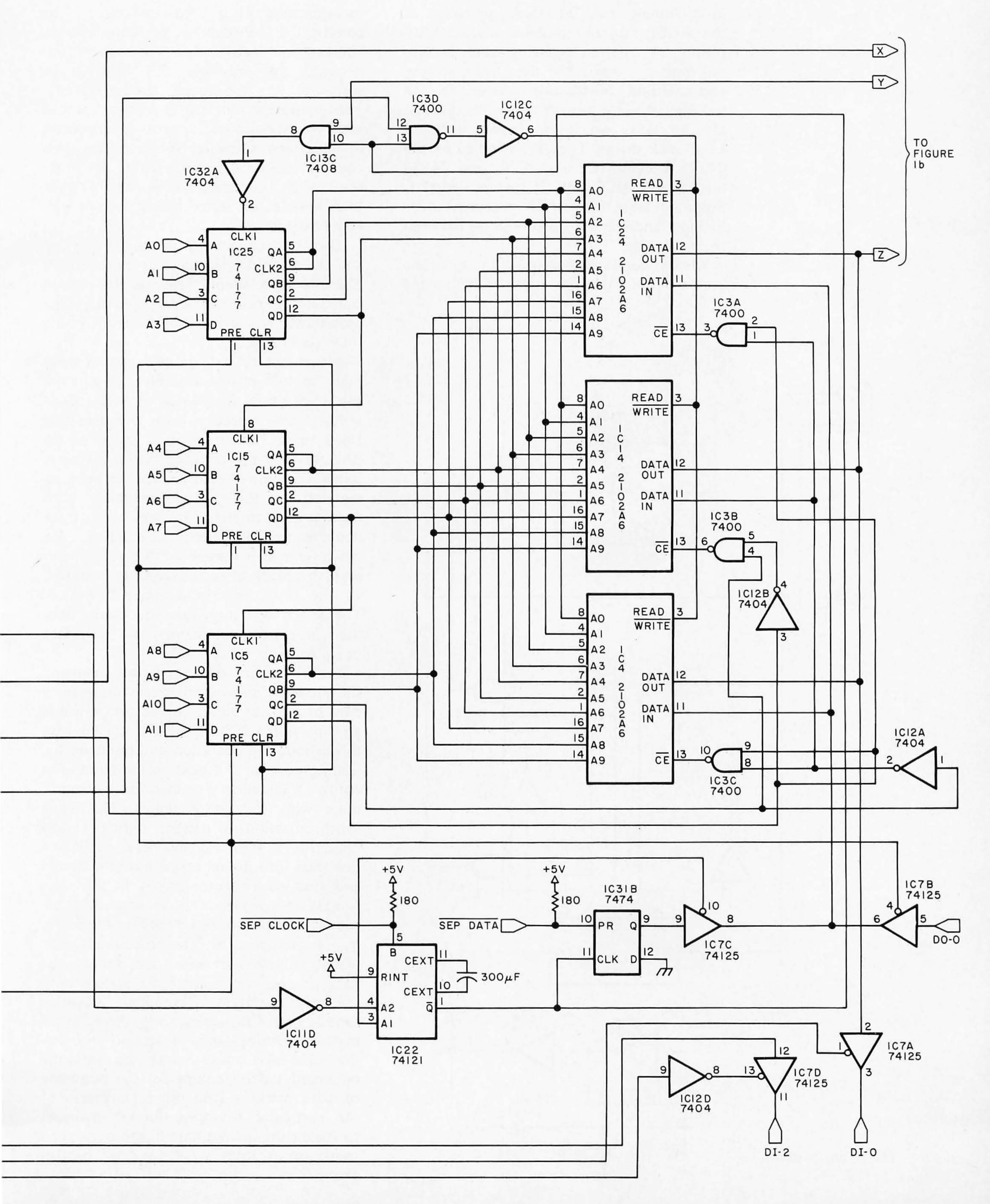
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Circle 56 on inquiry card.

Figure 1a: Schematic diagram for the floppy disk interface board. All inputs and outputs are designed and buffered for use with a Motorola 6800 processor and a Memorex 651 floppy disk drive.




X
Y
Z
TO FIGURE 1b
IC3D 7400
IC12C 7404
IC13C 7408
IC32A 7404
IC25 74177
IC15 74177
IC5 74177
IC24 2102A6
IC14 2102A6
IC4 2102A6
CLK1
CLK2
PRE CLR
READ WRITE
DATA OUT
DATA IN
CE
IC3A 7400
IC3B 7400
IC3C 7400
IC12B 7404
IC12A 7404
IC7B 74125
IC7C 74125
IC7A 74125
IC7D 74125
IC12D 7404
IC11D 7404
IC22 74121
IC31B 7474
+5V
180
300μF
SEP CLOCK
SEP DATA
RINT
CEXT
PR
CLK
DO-0
DI-2
DI-0
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11

in a floppy disk interface, regardless of the actual data transmission method. Outputting step pulses, receiving sector and index pulses, loading the data head, sensing and resetting the file unsafe error bit, and sensing the write protect tab on the diskette are functions which are largely universal to all disk drives. They are handled by the 74175 latches (IC2 and IC20) and 74125 bus drivers (IC6 and IC16) in figure 1. Software takes care of all necessary interlocking and timing relationships between these signals.

One minor exception is in the use of the sector pulses from the drive. I felt that the incorporation of a hardware counter (to convert the individual sector pulses into an address and relieve the processor of the necessity of providing this function in software) was too simple to be left out. The equivalent function in software would yield an excessive and unnecessary overhead in time and software. As such, the two counter packages, which provide the processor with a complete sector address rather than a series of sector pulses, were a welcome expense.

Data passage between the buffer memory and the disk drive is processor independent. The processor simply requests the desired transaction (read or write). Actual data movement is carried out solely by the interface circuits.

Movement of data in this system takes place in two phases, regardless of whether the transaction is a write or read. When writing, the processor loads the data destined to be recorded onto a sector of the diskette into the onboard buffer memory. When the entire sector's data has been assembled in this buffer, complete with necessary preambles, data separators, track and sector identifiers, postambles, and whatever else is needed by the chosen format, this block of sector data can be moved to the disk drive in a single operation. The actual operation does not occur until the processor commands the interface board to write.

After receipt of the write command the interface waits until it sees the leading edge of a sector pulse. This sector pulse sets a flip flop, IC30B, which remains set throughout the operation and resets on the leading edge of the next sector pulse. The entire transaction is therefore synchronous with the sector pulses. This same synchronization is present during a read operation as well. For example, reading of disk data into the on board buffer is started and stopped by sector pulses. In this way, format independence is accomplished because the entire sector is read into the buffer in a single operation. The processor is completely uninvolved with this transfer of data. It does not re-enter the picture until the read operation is complete, at which time it begins dissecting the received information. During this dissection process, the processor must search through the on board buffer looking for the beginning of data markers (and other landmarks of the particular recording format involved) to locate the desired data in the buffer and transform it from serial to 8 bit parallel form.

Figure 1b: Continuation of figure 1a.



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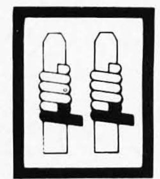




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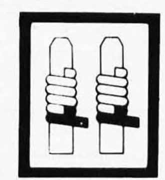


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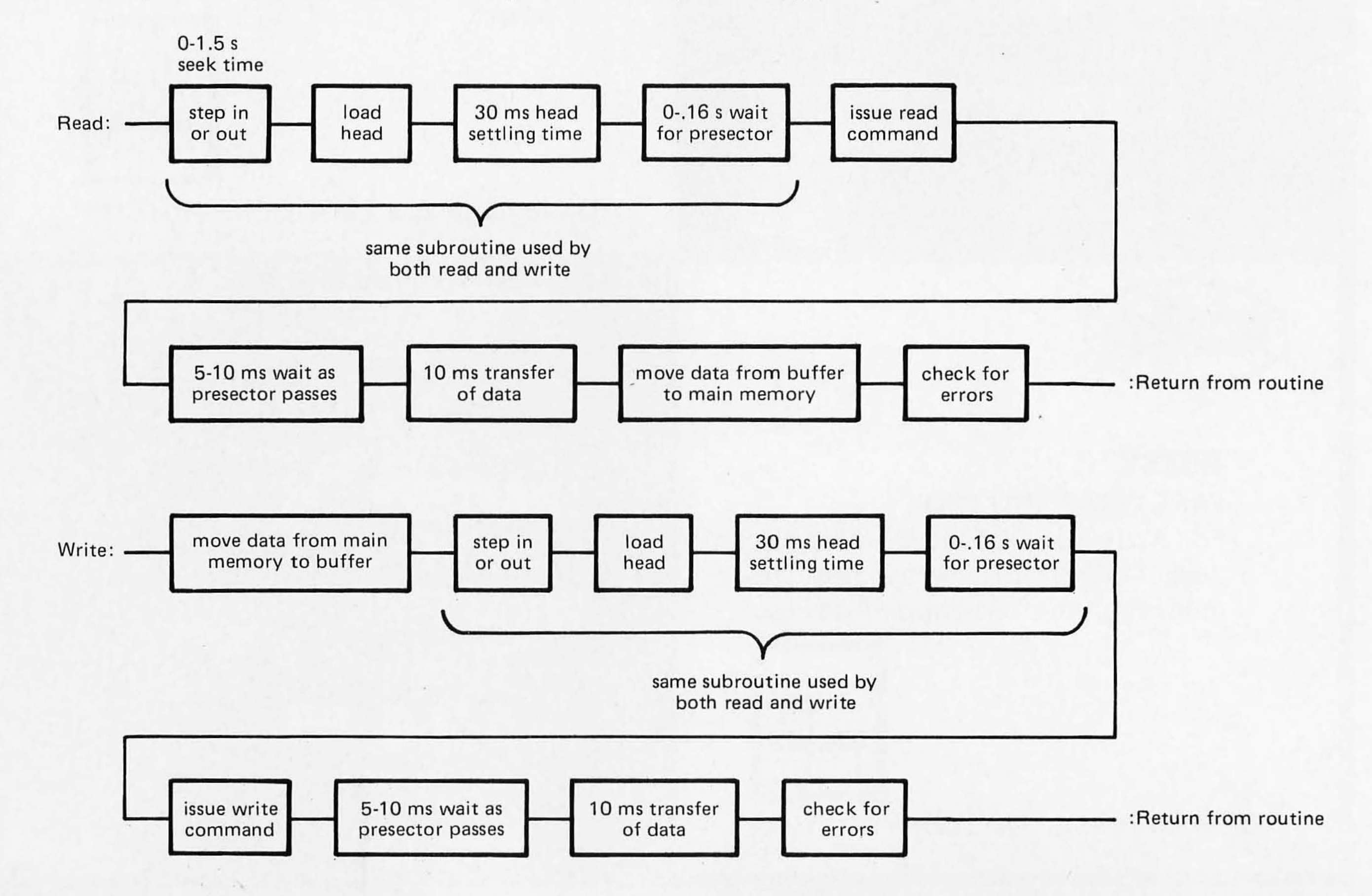
Note that, in this system, the actual SECTOR pulses from the disk drive are not used to start and stop the transactions; rather, they are divided by 2 in the first stage of the sector address counters. This means that although 32 physical sectors could be recorded per track on the diskette, this system will record only 16.

Each sector contains 256 bytes of data instead of 128. I did this to facilitate future double-density operation. The size of the buffer is 256 bytes of data plus some extra for preambles, checksums, and so on, for both single or double density operation. Only the number of sectors per track will be charged: they will increase from 16 for single density to 32 for double-density. For purposes of this article, single density operation is assumed.

The interface board knows nothing about the particular recording format involved, but merely collects a sector's worth of information (ie: everything appearing between two successive sector pulses) from the disk drive and gives it to the processor. The processor must know all about the organization of the data in the sector. The software completely controls the organizing and formatting of this data.

Although it is feasible to configure the buffer memory as an 8 bit wide parallel buffer, the serial configuration has several advantages including the lowest cost and chip count. It also permits efficient utilization of low cost memory chips such as the 2102A. Although it would seem logical to use serial shift registers for the buffer, doing so destroys the processor's ability to randomly access the buffer. Another reason for using serial data transmission is that conversion to parallel format, when receiving data from the disk, would necessitate some form of data synchronization information so that the packing of the serial data into the parallel buffer can be coordinated. Without this information, bit 1 might end up in bit 8's location. This synchronization function must be provided in any case. Postponing the problem until a time when the processor is processing the data, instead of the time when the disk drive and interface are exchanging data, allows the interface hardware to be format independent. This means that, with little

Figure 2: Sequence of main events when reading from or writing to the floppy disk.



or no change to the interface board, any hardware sectored format can be accommodated by the use of appropriate software. With the present amorphous state of the home computing industry, format independence has to be a significant advantage.

In figure 1, the three 2102As (ICs 4, 14 and 24) form a 3072 by 1 bit buffer memory. The three 74177 counters (ICs 5, 15 and 25), which are associated with the three 2102As, allow storage of the serially accessed disk data in the randomly accessed memories. These counters are incremented for each bit of disk data passed, and provide addresses for the 2102As during both the read and write operations. During reading, the disk provides clocking information in the form of SEP CLOCK on the Memorex disk drive. SEP CLOCK is used to clock the counters and address the memory. During writing, the interface card must provide clocking information to the disk. The crystal oscillator provides this write clock information for the disk drive as well as for the counters which address the memory.

The preceding has explained the functioning of the counters and the addressing of the 2102A buffer during data exchanges between the disk drive and the interface card. Movement of data between the interface card and the processor takes place before or after the interface's dialogue with the disk drive, as shown by the sequence of operations for read and write commands in figure 2. During this processor activity, the address counters take on a completely different function. The processor can randomly access any bit in the memory buffer. Therefore, the address for the buffer comes from the processor rather than from the address counters.

During this time, the addresses on the processor's bus, which are present at the preset inputs of the 74177s (ICs 5, 15, 25), are gated through to the 2102As. When the processor attempts to read from or write to the buffer it will be accessing only one bit at a time, since the buffer is only one bit wide. The 6800's read and write line is gated directly to the read and write line of the 2102As. Write data from the processor will be fed to the data input lines of the 2102As via a three state device enabled by the proper address decoding from the processor bus (IC1). When the processor reads from the buffer memory, address decoding (IC1B) enables a three state bus driver and places one bit of data from the buffer on the processor bus.

During a diskette read operation, it is desirable to use the received clock to strobe the received data into memory. In order to satisfy the minimum write pulse width requirements of some 2102 type programmable memories, it is necessary to use a oneshot (IC22) triggered by the trailing edge of the receive clock to generate the actual write strobe. The received data is latched in a 7474 (IC31B) and maintained until the end of the write strobe. Note that while it would normally be poor practice to use the write strobe to change both address and data, the architecture of this interface and of most 2102 type programmable memories permits this. The actual value of the address present at the edges of the write strobe appears to be irrelevant, provided that the address is stable. In this design, the address and the data change after the trailing edge. This arrangement has been tested with several types of programmable memories, from fast new ones to slow obsolete ones. There were no problems in any instance.

During a write operation, a 4 MHz crystal provides clock pulses to the disk drive and address counters for the 2102As. A 4 MHz crystal is used to facilitate the future double density option. A 2 MHz crystal could be used for standard density operation with the proper circuit modifications. The write clock and write data signals (outputs of IC17 and IC28B) are combined into a composite clock and data signal and fed to the disk drive via three paralleled sections of a 7416 high power inverter (ICs 10A, B, and C). Three sections are used to provide adequate signal current into the low impedance line receiver within the disk drive. Although line receivers are recommended by Memorex for the received clock and received data signals at the interface, standard TTL inputs (with the addition of the pull up resistors shown in the schematic) have proven to be adequate.

Software

The schematic of figure 1 does not represent a floppy disk controller, but only an interface. The processor intelligence is needed to make the system a controller. The bulk of the effort in establishing a system of this type occurs in the writing of the necessary software. This approach keeps the hardware costs low and allows the frugal experimenter to substitute his or her own software writing ability for the out of pocket hardware expenses.

Two phases in any read or write operation of the system were previously mentioned. A third phase is necessary prior to any actual reading or writing. The disk drive's data transfer head must be stepped

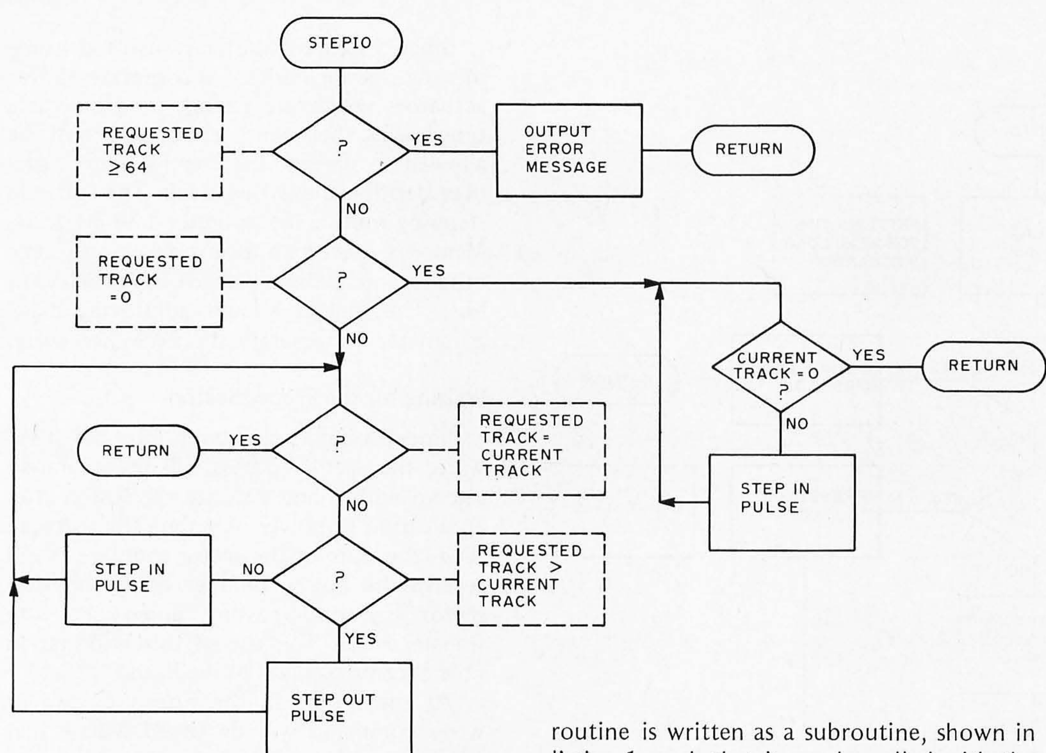


Figure 3: The stepping routine, which moves to any track that is requested.

to the proper track. Then the system must interrogate the hardware's sector address counters in order to know when it is permissible to issue a read or write command.

Stepping to the Proper Track

There are either 64 or 77 tracks on floppy disk systems (the Memorex 651 uses 64). When power is first applied to the system, the position of the data transfer head is unknown. It is necessary to find over which track the head is positioned. Unfortunately the disk drive tells us nothing about the location of the head unless it is sitting at the very first track of the system (track 0). Some disk drives have an additional sensor at the very last track. Consequently, during initialization of these systems it is necessary to step the data transfer head in toward track 0 until the track 0 sensor is tripped. If track 0 is requested (as shown in the flowchart of figure 3 for the stepping routine), the program will step the data transfer head in, while searching for a TRACK 00 signal. An 8 bit register remembers where the head is located. Once the head is stepped away from track 0, the software has no way of determining what track is currently accessed unless it knows how many step pulses have been issued. Every time a step pulse is issued, this counter will be incremented or decremented appropriately unless the track 0 signal appears, in which case the counter is cleared. This step routine is written as a subroutine, shown in listing 1, such that it can be called with the desired track parameter passed as a value in another register.

Stepping takes place in response to individual pulses from the interface. The pulses are formed in software by turning a hardware bit on, and then off. The width of the pulse will be determined by the processor's execution speed. Since two or more instructions are involved, the width will be several microseconds. Several NOPs can be inserted in the software as a safety measure.

Listing 1: Stepping in or out routine written for the Motorola 6800 processor.

```
FA3D B6 A055 STEPIO LDA A  REQTRK
FA40 81 3F          CMP A  #63
FA42 2F 03          BLE    *+5
FA44 7E FB8F        JMP    ADRERR
FA47 81 00          CMP A  #0
FA49 26 0F          BNE    STP2
FA4B C6 80   STP1   LDA B  #$80     TEST TRACK ZERO BIT
FA4D F5 9C00        BIT B  $9C00
FA50 27 04          BEQ    *+6
FA52 8D 1D          BSR    STEPIN
FA54 20 F5          BRA    STP1
FA56 7F A054        CLR    ACTTRK   TRACK ZERO FOUND
FA59 39             RTS
FA5A B1 A054 STP2   CMP A  ACTTRK
FA5D 26 01          BNE    *+3
FA5F 39             RTS
FA60 2B 04          BMI    *+6
FA62 8D 06          BSR    STPOUT
FA64 20 F4          BRA    STP2     LOOP TILL TRACK ZERO FOUND
FA66 8D 09          BSR    STEPIN
FA68 20 F0          BRA    STP2
FA6A 7C A054 STPOUT INC    ACTTRK
FA6D C6 01          LDA B  #1       STEP OUT PULSE
FA6F 20 05          BRA    STP4
FA71 7A A054 STEPIN DEC    ACTTRK
FA74 C6 02          LDA B  #2       STEP IN PULSE
FA76 F7 9C00 STP4   STA B  $9C00    BEGIN STEP PULSE
FA79 5F             CLR B
FA7A 01             NOP             DELAY
FA7B 01             NOP
FA7C F7 9C00        STA B  $9C00    END STEP PULSE
FA7F CE 0C00 DELAY  LDX    #$C00
FA82 09      STP3   DEX
FA83 26 FD          BNE    STP3
FA85 39             RTS
```

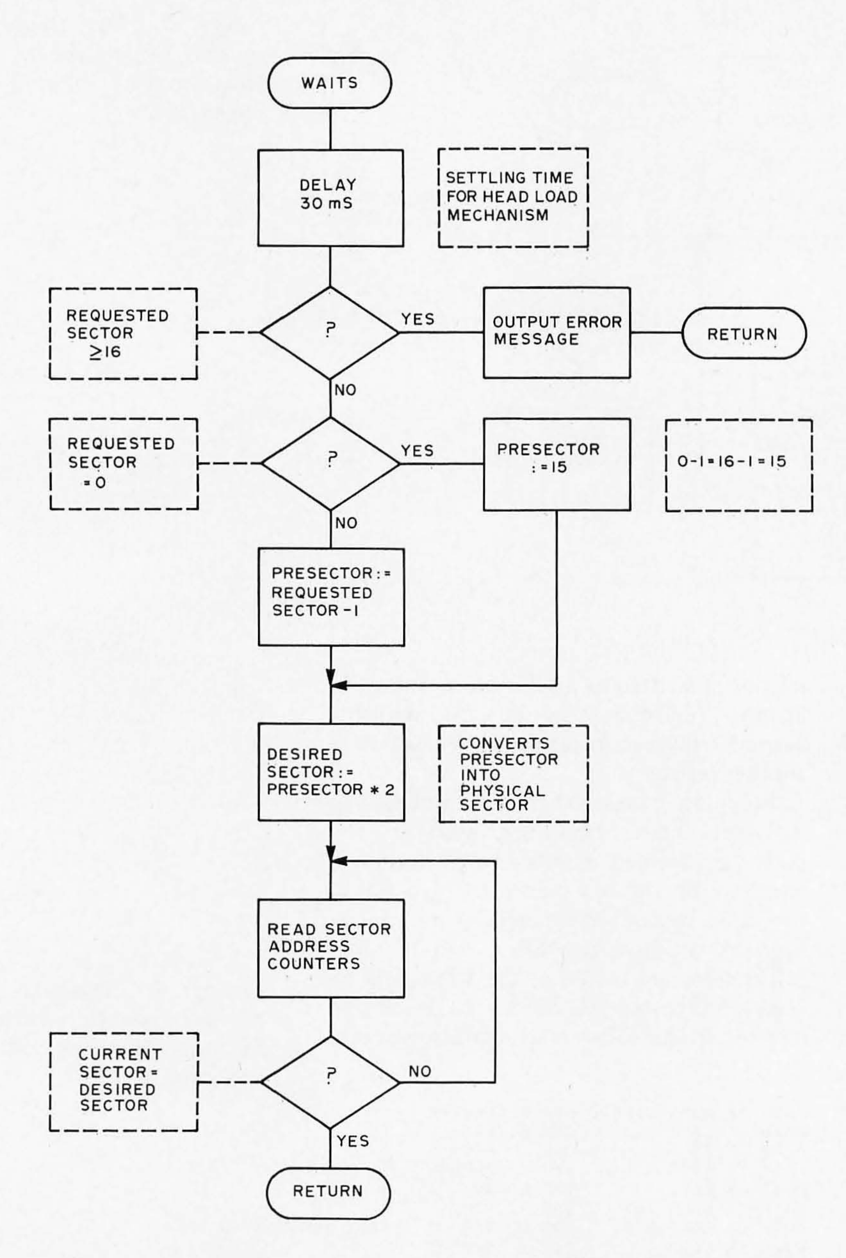


Figure 4: A routine which searches a single track until it finds the required presector.

```
FAA4 8D D9    WAITS  BSR     DELAY
FAA6 B6 A051         LDA A   REQSEC
FAA9 81 10           CMP A   #$10     IS REQ'D SECT. LEGIT.?
FAAB 2D 03           BLT     WS1
FAAD 7E FB8F         JMP     ADRERR
FAB0 81 00    WS1    CMP A   #0       SECTOR 0 REQ'D
FAB2 26 02           BNE     WS2
FAB4 86 10           LDA A   #$10     DUMMY SECTOR #
FAB6 4A       WS2    DEC A            SET UP PRESECTOR
FAB7 48              ASL A            SET UP HARD SECTOR NUMBER
FAB8 F6 9C00  WS3    LDA B   $9C00    GET SECTOR FROM INTFC
FABB C4 1F           AND B   #$1F
FABD 11              CBA              REQ:ACTUAL
FABE 26 F8           BNE     WS3
FAC0 39              RTS
```

Listing 2: Interrogation routine written for Motorola 6800. This routine checks each of the sector headings on a track until it finds the requested presector of the desired sector.

Since a stepping motor is involved (some of the newer drives incorporate linear actuators which are faster), a considerable time delay between step pulses must be allowed to prevent the stepper motor from overshooting the wrong track. The software stepping routine incorporates a 30 ms delay. Memorex specifies a 20 ms delay, and some other manufacturers call for 10 ms delays or less. The builder should adjust the delay parameter to generate the necessary delay.

Waiting for the Proper Sector

Since counters are built into the hardware, the sector address will be accurately known within one diskette revolution after application of power. Anytime the software reads the state of the sector counters, it will receive the binary number of the physical sector currently passing under the data transfer head. The use of this information now becomes somewhat involved.

At some time in the future, a read or write command will be issued. Where that occurs is a function of the time when the command is issued relative to the position of the diskette at the moment of issuance. If the user wants to write at logical sector 4 of the current track, for instance, the write command is issued prior to the appearance of physical sector 4 beneath the data transfer head. In other words, the command should take place while the data head is over sector 3 because the actual writing must begin at the leading edge of the sector pulse that introduces physical sector 4.

Things are actually more complex than this. The counters which address the on board buffer memory must be reset prior to the beginning of the actual read or write operation. Otherwise, the buffer addresses would begin in the middle of the buffer. In order to guarantee sufficient time for resetting the counters, some finite time interval must occur during the preceding physical sector. The only way to insure this is to locate the end of second preceding physical sector and issue the read or write command at the beginning of the immediately preceding physical sector.

The flowchart in figure 4 shows a subroutine which, when given the desired sector to be read from or written to, will loop while interrogating the sector counters until the presector is found. Although the software of listing 2 appears to ignore the need to guarantee some resetting time for the buffer address counters, this is not the case. Since there are two physical sectors for each logical sector (32 physical sectors per track versus 16 logical sectors) the software is sensing

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```
F9BB FF A05E READSV STX     DBUFF     SAVE DATA DESTINATION ADDR
F9BE BD FA86        JSR     MSETUP    MOVE HEAD TO TRACK/SECTOR
F9C1 86 03          LDA A   #3
F9C3 B7 9C01        STA A   $9C01     REQUEST READ
F9C6 BD FA95        JSR     WAITFL    WAIT FOR 'FINISHED' FLAG
F9C9 BD FB08        JSR     ENPACK    CONVERT DATA TO 8-BIT BYTES
F9CC BD FB66        JSR     CHKSUM    COMPUTE NEW CHECKSUM
F9CF FE A05A        LDX     CKSM
F9D2 BC 5100        CPX     RBUFF+256  COMPARE NEW WITH RECORDED
F9D5 27 03          BEQ     *+5
F9D7 7E FB87        JMP     CKSMER
F9DA FE A056        LDX     REQADR    ADDR REQ'D BY CONTROLLER
F9DD BC 5102        CPX     RBUFF+258  COMPARE W/RECORDED ADDR
F9E0 27 03          BEQ     *+5
F9E2 7E FB99        JMP     TSIDERR
F9E5 CE 5000        LDX     #RBUFF
F9E8 FF A05C        STX     SBUFF
F9EB BD FA26        JSR     COPY
F9EE 39             RTS
F9EF FF A05C WRITSV STX     SBUFF     X-REG DESIGNATES SOURCE DATA
F9F2 C6 20          LDA B   #$20      TEST WRITE PROTECT
F9F4 F5 9C00        BIT B   $9C00
F9F7 26 03          BNE     *+5
F9F9 7E FB9E        JMP     WPROT
F9FC CE 5000        LDX     #RBUFF
F9FF FF A05E        STX     DBUFF
FA02 BD FA26        JSR     COPY
FA05 BD FB66        JSR     CHKSUM    COMPUTE CHECKSUM
FA08 FE A05A        LDX     CKSM
FA0B FF 5100        STX     RBUFF+256
FA0E FE A056        LDX     REQADR
FA11 FF 5102        STX     RBUFF+258
FA14 BD FAC1        JSR     UNPACK    STORE ASSEMBLED FILE
            *                         INTO SERIAL BUFFER
FA17 BD FA86        JSR     MSETUP    POSITION HEAD, ETC.
FA1A 86 02          LDA A   #2        WRITE TRANSACTION
FA1C B7 9C01        STA A   $9C01
FA1F BD FA95        JSR     WAITFL    WAIT TILL DONE
FA22 BD FB3D        JSR     CHKFIL    CHECK FILE UNSAFE
FA25 39             RTS
```

Listing 3: The WRITSV routine allows writing to the disk, and the READSV routine is used to read data from the disk. When either of these two routines is entered, the correct track and sector have been found and the data transfer head is already loaded and allowed to settle.

physical sectors and dividing the sensed addresses by 2. This will allow at least 5 ms (the time for one physical sector) for resetting the address counters.

Read and Write Commands

One bit of a status word is used to identify a read or write command. In the schematics, logical 1 means *read* and logic 0 means *write*. Another bit is used as the transaction request bit. Setting this byte to logical 1 enables the hardware to execute a data transaction when the next sector pulse occurs. During this period of time the processor must not read from or write to the on board buffer, since this will immediately set the address counters to the value present on the processor's address bus. The processor needs to know if the disk drive is talking to the buffer memory. Therefore, a busy or ready bit is incorporated into the hardware. Proponents of interrupt driven systems should note that a separate flip flop is set at the end of a read or write transaction. This should be reset in software prior to issuing a new command. Hardware will reset the flip flop automatically at the beginning of each transaction in the event that software does not do this. This flip flop can be used as a flag for a testing loop, or it can be tied to an interrupt line to generate an interrupt upon completion of the read or write transaction. The software examples used here incorporate a flag testing loop routine.

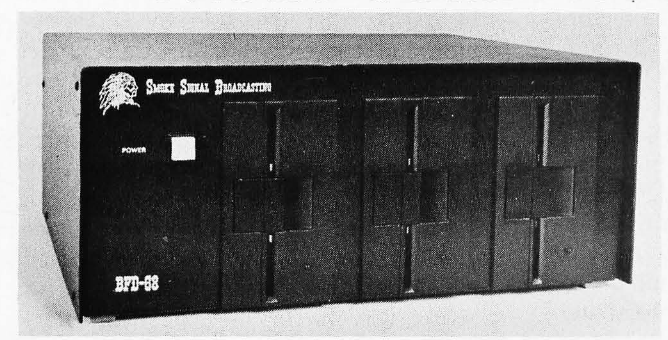
Operating Sequence

Sometime prior to the passing of the data to or from the disk drive, the head load bail must be energized to permit the data transfer head to come into contact with the diskette. The mechanical properties of this mechanism dictate that some time must be allowed for settling prior to the commencement of any data movement. Various philosophies exist on the subject of how long and how often the head should remain loaded. Some feel that the head should be loaded continuously during periods of usage, and that frequent loading and unloading of the head causes aggravation of the head as well as a media wear problem. The software I use assumes just the opposite: The less time the head and media are in contact, the less wear will occur. Memorex drives are particularly vulnerable to wear, since they use metal heads instead of newer ferrite and ceramic heads. A Memorex drive using this software and operating in a suitably clean environment for several months has had no detectable wear to either the data head or the diskette. I feel that this is due to the fact that the data head is never in contact with the media for more than a fraction of a second at a time. The accumulated contact time is kept very low.

In the software of listing 3, the data head is loaded just after the stepping routine, immediately following the arrival at the proper track. Recall that the system will begin its search for the pre-presector after the proper track has been accessed. The sector wait algorithm contains a 30 ms delay during which the head load mechanism can settle. An extra delay loop should be inserted at the entry of the sector wait routine if additional settling time is necessary. The accumulated system delay, including the sector wait routine, will probably be adequate.

Figure 5 shows the sequence of operations for read and write commands and includes the movements of data relative to the mechanical operations. For a clearer description, see photo 1. If a wire operation is to take place, the first step in the process should be setting up the data in the interface's onboard memory buffer. Some sort of structure must be chosen for the various

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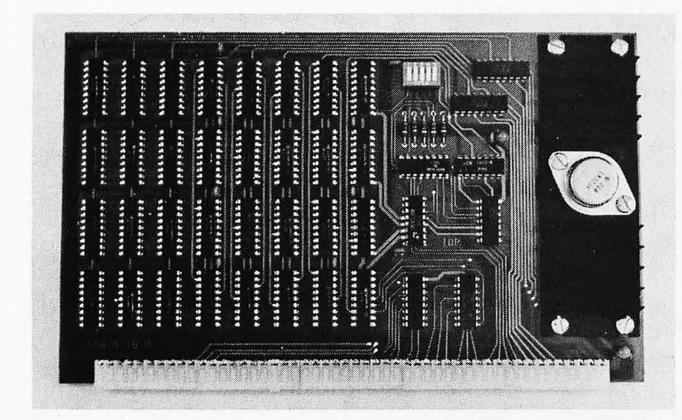


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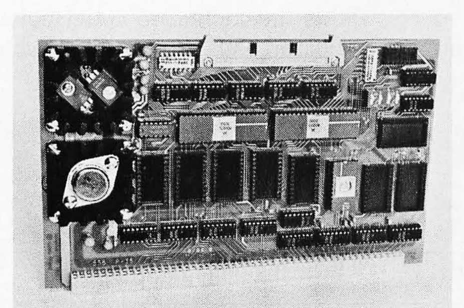
The BFD-68 includes our Disc Operating System Software. The software provides direct commands to name and rename files, transfer memory to disc and disc to memory and to automatically jump to the starting location of any program loaded from disc to memory. The direct command names are: RUN, GET, GETHEX, CLOSE, SAVE, DELETE, APPEND, RENAME, COPY, LIST, LINK and PRINT. In addition, the Disc File Management subroutines are available to create files under your program control.

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zones which must be recorded onto each sector. Memorex recommends that a preamble of 128 logical 0s be written to the disk starting at the beginning of the sector. What goes onto the disk after that is dependent on the whims and opinions of the programmer. In the prototype system, a single logical 1 follows the preamble and serves to indicate that the next following bit is the first bit of the first word of data. 256 8 bit words are then written with the least significant bit first. This is followed by a 16 bit checksum, a 16 bit binary number to indicate the sector and track numbers, and zeroes for a postamble, which will end when the hardware encounters the sector pulse for the next sector. I make no claims for the elegance or efficiency of this format. It was expedient and has worked for months in a small developmental system. To set up the on board buffer with this information, a routine converts the source data from 8 bit parallel to serial (1 bit per address) in the buffer. After the buffer is set up, the mechanical movements and commands can be issued.

Operating

If the interface is wired correctly with properly working parts and the software is bug free, the system should work without any adjustments. However, if you build the hardware and write the software from scratch, there are many chances for error. I highly recommend that you build and test one section at a time. When testing the data circuits, a good quality oscilloscope, preferably dual trace with delayed sweep, is desirable. The read and write operations are conducted independent of the processor. This simplifies troubleshooting because bad software will not complicate the situation.

I suggest that you start by wiring the sector counters and verifying their proper operation by reading sector addresses into the processor. Once the sector counters are working, the sector wait software can be written and tested by observing the varying time that the software is tied up (by looking for the desired sector). This varying time is formally known as the rotational latency, and will be between 5 and 160 ms.

Next, wire the step in, step out, and track 00 signals. The stepper motor can be manually tested by shorting the stepping lines to ground. It is much more dramatic to write some simple software to exercise this function. At this time the stepping speed can be set and the malfunctioning of the stepper motor can be observed at excessively high step rates.

The first step in testing the operation of the on board buffer memory is to transmit data back and forth between the interface and the processor. Doing so will bypass the oneshot, address counters, etc, and make testing much simpler. Once the memory is found to be functional, communication with the disk can be tested. Grounding pin 11 of IC30B will force the hardware to execute a continuous string of read or write commands depending on the state of flip flop 31A. Flip flop 31A can be used to choose either read or write commands. When writing, the normally present reset signal at the timer counter (pin 13 of IC26) will be lifted. This allows the counter to count pulses from the oscillator. Pulses from the clock gate, pin 6

Figure 5: Timing diagram for read and write operations. Also shown is the physical and logical layout of the data on the floppy disk.

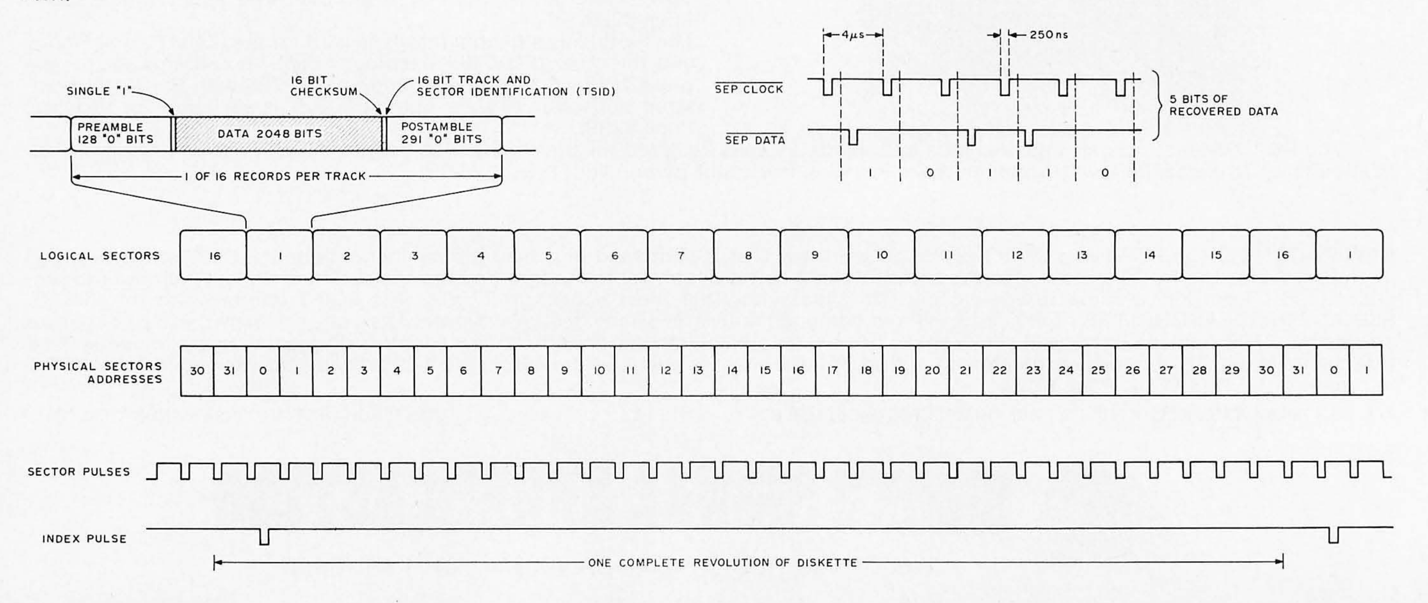


Photo 1a: Data as it appears when first received from the disk drive for eventual storage in the buffer memory.

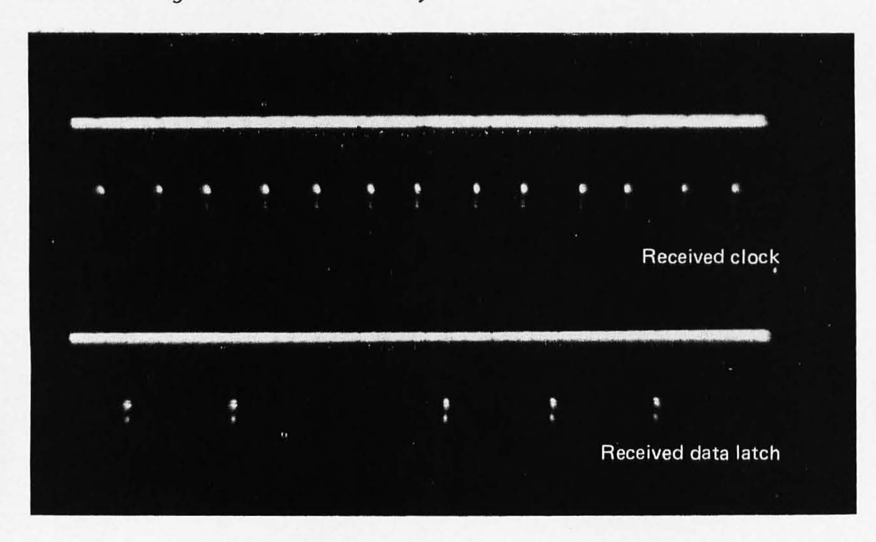
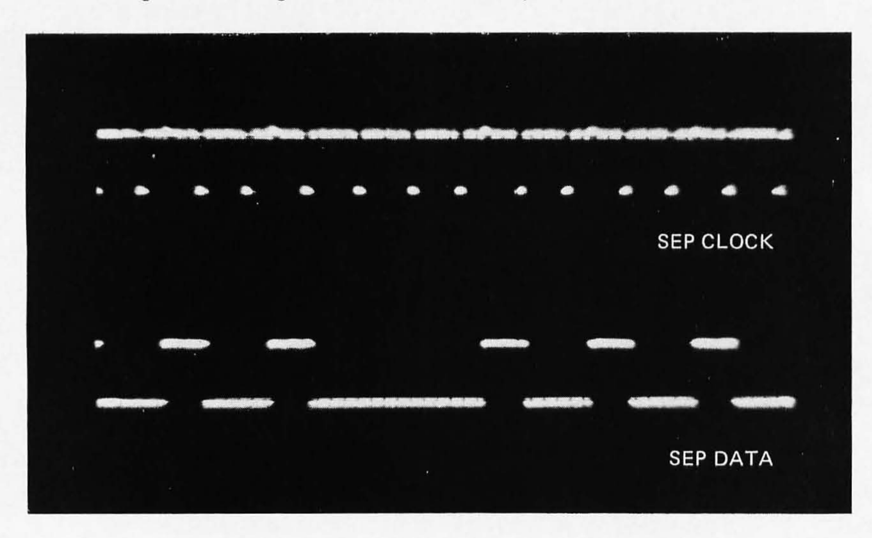


Photo 1b: An example of data which has been received from the disk drive and rearranged for storage in the buffer memory.



of IC28A, will be a continuous stream of pulses separated by 4 μs. Pulses from the data gate, pin 8 of IC17, will be dependent on the raw data coming from the 2102As. If the raw data is a steady high, the signal from the data gate will be similar to that from the the clock gate with the exception that the two signals will be displaced in time. When the two signals are combined at pin 8 of IC28B, they are interleaved. While the interface is in forced write mode, the clock pulses from the clock gate are applied to the address counters, pin 8 of IC25. These counters should be counting properly. Whatever data is stored in the 2102As should be coming out serially on the raw data line.

To test the read function, you will need a working disk drive and a prerecorded diskette. With the head loaded, a stream of data and clock pulses similar to those observed in the write circuits should be present at SEP CLOCK and SEP DATA. The one-shot should fire (pin 1 of IC22) on the trailing edge of each clock pulse. The one-shot's output should appear at the address counter's input and at the read and write line of the 2102As, pin 3 of ICs 4, 14 and 24. The 1 bit SEP DATA latch IC is set at the leading edge of any SEP DATA pulse and reset by the trailing edge of the one-shot's output.

The only other circuit of any complexity is that of the interrupt flag. If a read or write operation is terminated normally by the occurrence of the second sector pulse at the "busy" flip flop (pin 11 of IC30B), then resetting the flip flop will clock the interrupt flip flop on (pin 9 of IC27B) and either generate an interrupt or be used as a flag. This interrupt flip flop will remain on until software clears it by setting the interrupt clear flip flop, or until hardware clears it as soon as the transaction request flip flop, pin 6 of IC30A, is set in preparation for another read or write operation.

All other circuits are address decoding, latching, or bus driving functions and do not bear explanation here.

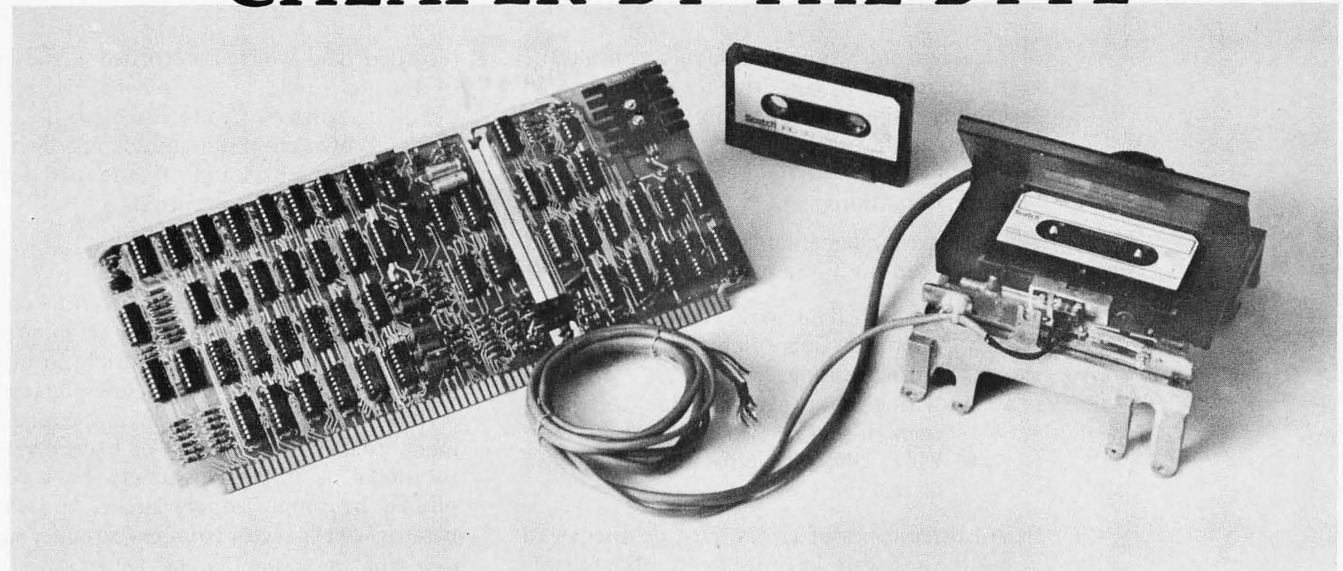
Drive Power

The lowly power supply is usually the least considered element in a system until it has to be paid for or fixed. Most floppy disk drives are extremely inefficient, due principally to the stepper motor. In the Memorex design the stepper motor consumes 24 V at 2 A. I have had only one troublesome power supply problem. It turned out to be due to an induced transient caused by a snapping action in the rectifier diodes during recovery and turn off. The resultant noise caused problems everywhere. I solved this by simply shunting the diodes with .05 or .1 μF capacitors.

Intercabling

Memorex offers a version of its drive for use with twisted pair signal lines and a printed circuit edge connector in place of the 93 Ω coaxial cable and captive pin connector of the original. This newer version should definitely be specified when buying from Memorex. For intercabling of six to eight feet between the interface card and the drive, twisted pairs will be adequate and virtually any connector will suffice. Each twisted pair should consist of a signal wire paired with a ground wire and have one or two twists per inch. If you have a high

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  254,000 8-bit bytes on C-30 cassettes
  508,000 8-bit bytes on C-60 cassettes
- Software error rate less than 1 bit in 10^8

What our system allows you:

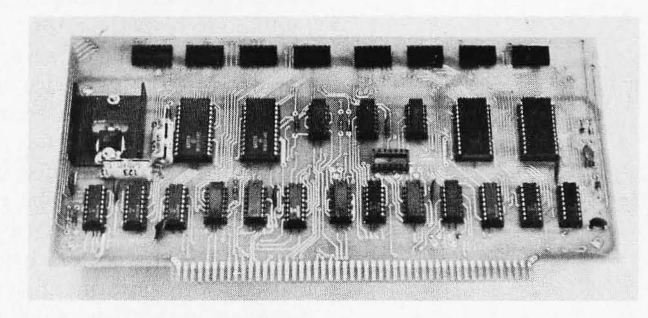
- Indexed software controlled program file
- Indexed random retrieval
- Multipass compilers
- Duplication and backup of important data
- Large data files — lists, names, business accounts
- System residence

What our software operating system offers:

- 8080-based design
- Cyclic redundancy check (CRC) error detection
- System retries after soft errors
- Automatically bypasses hard errors
- Block size from 1 to 256 bytes or 256-byte increments
- Phi Deck Monitor Operating System

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Address ______________________
City/State/Zip ______________________

density application you should consult the manufacturer of the drive for recommended cabling, since comparatively high speed signals are involved.

Error Conditions

Three fundamental types of errors should be allowed for in the system:

- Desired data not accessible due to improper recording, dirt, or noise during reading.
- Wrong data accessed due to wrong track or sector.
- FILE UNSAFE error flagged by disk drive.

All three types of errors must be discovered by the software in order to establish reliable operation.

The FILE UNSAFE error is probably the most common type encountered. It typically results from attempting to write to a write protected diskette or attempting to write while the door of the drive is open. Malfunctions of the electronics within the disk drive will also cause a FILE UNSAFE error. These are quite rare, at least in Memorex drives. Since this type of error is typically due to the operator, Memorex recommends that manual intervention be required to reset the error condition.

Accessing wrong data because of being on the wrong track or sector will occur if the step rate of the pulses formed by the stepping software is too fast for the stepper motor or if electrical noise causes the sector counters to miscount. This type of error can only be detected during a read operation, and only if the sectors being read are formatted with information describing their intended physical location on the diskette. This is the purpose of the track sector identification (TSID) word included with each record written to the disk. When the record is read, the track sector identification is checked to see if it agrees with what was supposed to have been read. If it does not, an error has occurred. In practice this type of error should never occur unless there is some serious malfunction due to faulty design, improper operation, or bad software. In my prototype software, all operations halt when this type of error occurs and the operator is required to restart it.

The first of the three errors listed above is supposedly the most common. In my experience, though, it is quite rare *if* the drives and diskettes are kept clean and operated properly. The error is detectable by virtue of the checksum, a binary sum of all bytes of recorded data which is recorded at the end of the data field in the record. When the operating software reads a sector, it computes its own checksum and compares it to the recorded checksum. If the two sums disagree, an error has occurred.

Improvements

Since one step has already been taken in making the interface useful in an interrupt driven system, it might be sensible to make the interface more completely interrupt driven. In other words, eliminate the requirement that the processor wait during the rotational latency. This could be accomplished by simply adding latches and comparators to the sector counters' circuitry such that the processor could issue a desired sector number and a read or write command, then go about its business while the comparators search for the proper sector and initialize the read or write operation. This feature would probably only increase the chip count slightly and might be a worthwhile addition to units used with sophisticated disk operating systems.

The design I've discussed has been furnished to Midwest Scientific Instruments Inc for manufacture under license. The addressing structure of the Midwest Scientific version differs from that shown in the schematic of figures 1 and 2 in that they added peripheral interface adapter (PIA) chips, through which all communication between the processor and the interface must pass. This does not change the fundamental operation of the system, but it does increase the chip count. Budget minded users with the ability to build their own hardware are advised to build their own system, since it is basically not very complicated.

As an aid to persons building their own systems, the complete software, excerpts of which are used in this article, consisting of a 1 K byte microdisk operating system, is available for $10 in source form for the 6800 processor. Send to David M Allen, 1317 Central Av, Kansas City KS 66102. This software is written to utilize the routines of MIKBUG™ and provides named files of assignable length. Persons interested in hardware and software systems based on the interface discussed here should contact Midwest Scientific Instruments Inc, 220 W Cedar, Olathe KS 66061, (913) 764-3273.■

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Some people build personal computers for the love of building. And the systems they buy are usually more fun to build than to operate.

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And the exclusive Noiseguard ™ system on our 20-slot busboard produces signals that are "textbook clean," eliminating a major source of data errors and interfacing problems that plague most other personal computer systems. Plus, there are dozens of other features to make your mainframe more convenient: carrying handle and tilt-up stand, key-operated power switch for system security, spare power regulators for your small peripherals, and more.

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Interfacing your input/output devices to your mainframe can be a frustrating, expensive and time-consuming process.

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The Equinox I/O Interface is a single board that plugs right into your Equinox 100™ bus. And you're ready to plug in 3 audio cassette units with individual motion control, a Teletype* or RS-232 terminal, and any 8-bit parallel device. . . including graphics display, line printer or paper tape reader.

The Equinox I/O Interface has 1K bytes of RAM and ROM on board, preprogrammed with powerful Cassette Operating Executive (COPE) software. COPE handles dozens of interfacing and data handling tasks to increase the efficiency of your software. Your programs can store and retrieve cassette data with a simple CALL COPE instruction. Data is formatted, checked and transferred in blocks up to 64K bytes with a single READ or WRITE instruction. COPE can even bootstrap your programs.



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All Equinox software is designed to make full use of COPE capabilities. So loading your Equinox software is as simple as selecting an address and pressing RUN. Cassette data storage has never been more convenient.

The Equinox I/O Interface is programmed for the highly-reliable 300 baud Kansas City Standard for cassette data transfers. . .but can be reprogrammed for faster rates in the future. Your TTY/RS-232 channel also features user-programmable rates up to 4800 baud. And you have access to all COPE routines.

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The Equinox System TM is the first system to offer the ECONORAM III TM 8K × 8 memory board with the advanced SynchroFresh TM natural-timing refreshing system.

Configured as two individually addressable 4K blocks, the ECONORAM III TM comes assembled, tested and guaranteed to work perfectly in your Equinox System TM for one full year. It is also available as a lower-cost kit.

For tight budgets, the K-Ration TM 4K × 8 static memory kit is also available for your Equinox System TM. This high-efficiency design is one of the most widely used, lowest power and lowest cost memories available for S-100 systems.

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The Equinox System TM now includes two primary software packages: EQU/ATE for text-oriented programming, editing and assembly, and BASIC-EQ language for number-oriented programming.

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EQU/ATE gives you the power of a fully programmable text language. Using EQU/ATE, you can create programs to edit copy, keep inventory, manipulate your files of addresses or recipes, and more.

EQU/ATE is also one of the most powerful editor/assemblers available. EQU/ATE writes, assembles and executes your programs. It is fully symbolic, accepts global symbols and assembles programs larger than available memory.

EQU/ATE is also an extraordinary text editor which works interactively with you to edit by character, string or line. It also offers full number editing of memory contents in octal, hex or decimal.

Yet, EQU/ATE is extremely compact, occupying only 4K of memory with 8K total memory required.

BASIC-EQ is a powerful, interactive, high-level programming language developed for math and science applications. Its primary use is in the manipulation of numbers, although it is capable of string oriented operation. Our version, BASIC-EQ, occupies 5K of memory.

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IN PERSON	**See The Equinox System TM at your local computer shop.**

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Continued from page 35

out paper, purchased programs, etc) which have limited life spans and were not included under *cost of goods sold and/or operations* in Schedule C-1.

Taxing Situations at Home

If you're working out of your home you may only claim deductions if some part of your home is used *regularly and exclusively* "(a) as your principal place of business, (b) as a place of business used by your patients, clients and customers in meeting or dealing with you in the normal course of your trade or business, or (c) in connection with your business if it is a separate structure that is not attached to your dwelling unit." [*Page 23 of the 1976 Federal Income Tax Forms package containing Form 1040, Schedules A and B, Schedule C, Schedule D, Schedule E, Schedules R and RP, Schedule SE, Form 2441. Dept of the Treasury, Internal Revenue Service.*] This means that if some portion of your home is used *solely* for business purposes on a regular basis, you can deduct a percentage of your light, heat, telephone, trash removal, and rent or house payment for it. Thus, if you use 15% of your house in this way, you can deduct 15% of each of the expenses listed. Some people figure their percentage on the basis of the number of rooms in the house (thus, if one room of a 5 room house is so used, 20% is deducted); but I prefer the floor space method, whereby 200 square feet out of 1000 total square feet of floor space must be used for business purposes to justify a 20% deduction. This method reduces the risk of challenge. Be wary of taking this deduction, however, since using the area in question for *any* nonbusiness purpose can make a deduction illegitimate. Also, since computer entrepreneurs are most likely to work on their businesses at irregular intervals, it may be impossible to claim that the area is used on a *regular* basis for business. If you can legitimately claim these deductions, however, they increase the total deductible business expense considerably.

Line 20, which is the result of all these entries and computations, shows the sum of all deductions (lines 6 through 19k). If this is larger than the sum on line 5 (*total income*), enter the difference, preceded by a minus sign on line 21 as net business loss. If it is smaller, again enter the difference on line 21, preceded this time by a plus sign, as your net business profit. In either case, enter the figure that appears on line 21, with its appropriate sign, on line 29, *business income or (loss) (attach Schedule C)*, of form 1040.

Schedule C-4, *expense account information*, probably won't apply to computer entrepreneurs. Only expense account allowances which, added to salary, exceed $25,000 need be entered.

Schedule SE

Schedule SE is for computing your social security self-employment tax. If you aren't making a profit above a certain amount (currently $400, subject to change by law) you don't have to pay social security tax; but it's advisable to fill out the form anyway, because it proves that you owe no social security tax.

As usual, there is a place at the top for your name, social security number and type of business. (See figure 3; Schedule SE has no printing on back.) Part I is for those engaged in farm self-employment. It doesn't apply to nonfarm people and can be ignored. Part II, for nonfarm self-employment, however, does apply. Fill in line 5a with the net profit or loss figure calculated for line 21 of Schedule C. Lines 5b, c, d and e probably will not apply. Line 6, the total of lines 5a through 5e, represents total nonfarm self-employment income. Some adjustments to your business income permitted in the figuring of Schedule C are not allowable in figuring your income for the purpose of Schedule SE; the latter are covered on line 7. These adjustments include, for example, net operating losses from a previous year, income of public officials, rentals received from certain kinds of real estate, and the like. They are not likely to affect computer entrepreneurs, so I only note their existence here and refer you to the IRS instructions for Schedule SE. Business income (or loss) plus these adjustments is shown on line 8.

The nonfarm optional method, lines 9 through 11, may be used by those who did make a net profit and whose profit is both less than $1600 and less than two thirds of their gross profit. It involves comparing two thirds of your gross nonfarm profit (or $1600, whichever is smaller) with $1600 and calculating your social security tax on the smaller amount. For most computer entreneurs, this won't apply, at least during the first few years.

Social security self-employment tax is calculated in part III. Enter your business profit or loss (from line 8 or line 11) on line 12b. Add to it (on line 12a) any farm earnings (probably 0 in this case) and add them on line 13. If the resulting amount is less than $400, you owe no tax and can stop filling in the schedule right there; if it is greater than $400, you must total your wages and tips, etc, subject to FICA (the

Federal Insurance Contributions Act) on lines 15a through 15c and subtract the total from the maximum amount subject to social security tax, which is shown on line 14. The result of this subtraction goes on line 16 and whichever amount is smaller, line 13 or line 16, goes on line 17 as the basis of your social security tax. In 1976, the maximum amount of earnings subject to social security was $15,300, and whoever had this much or more was required to pay $1208.70. The tax on any amount less than the maximum was computed by multiplying the amount by 0.079. These figures are subject to change, however, and should be used only as a general gauge of tax amounts.

Being Prepared

Most people begin their computer enterprises in the hope of picking up a little cash to help improve their home systems. They rarely bother to account for expenses, assuming that they would have "spent the money anyway," and they usually pay little heed to profits apart from spending them quickly for more or better computing equipment. But hobby income is taxable, and if one suddenly finds him/herself with a product or service that is selling like the proverbial hotcakes, he/she can also build up a hefty tax bill without realizing it. Similarly, if one doesn't record the expenses that the enterprise entails, a thousand dollars could easily be spent to attain an income of only $227. Either way, it can get uncomfortable.

Keeping even the most simplified records from the start will help solve these problems.

SCHEDULE SE (Form 1040)
Department of the Treasury
Internal Revenue Service

Computation of Social Security Self-Employment Tax — **1976**

▶ Each self-employed person must file a Schedule SE. ▶ Attach to Form 1040.
▶ See Instructions for Schedule SE (Form 1040).

- If you had wages, including tips, of $15,300 or more that were subject to social security or railroad retirement taxes, do not fill in this schedule (unless you are eligible for the Earned Income Credit). See Instructions.
- If you had more than one business, combine profits and losses from all your businesses and farms on this Schedule SE.

Important.—The self-employment income reported below will be credited to your social security record and used in figuring social security benefits.

NAME OF SELF-EMPLOYED PERSON (AS SHOWN ON SOCIAL SECURITY CARD): FARADAY JESSUP WINSTEAD
Social security number of self-employed person ▶ ***:**:****

Business activities subject to self-employment tax (grocery store, restaurant, farm, etc.) ▶ PROVIDE COMPUTER SERVICES

- If you have only farm income complete Parts I and III.
- If you have only nonfarm income complete Parts II and III.
- If you have both farm and nonfarm income complete Parts I, II, and III.

Part I — Computation of Net Earnings from FARM Self-Employment

You may elect to compute your net farm earnings using the OPTIONAL METHOD, line 3, instead of using the Regular Method, line 2, if your gross profits are: (1) $2,400 or less, or (2) more than $2,400 and net profits are less than $1,600. However, lines 1 and 2 must be completed even if you elect to use the FARM OPTIONAL METHOD.

REGULAR METHOD 1 Net profit or (loss) from: a Schedule F, line 54 (cash method), or line 72 (accrual method)	1a		
b Farm partnerships	1b		
2 Net earnings from farm self-employment (add lines 1a and b)	2		
FARM OPTIONAL METHOD 3 If gross profits from farming[1] are: a Not more than $2,400, enter two-thirds of the gross profits; b More than $2,400 and the net farm profit is less than $1,600, Enter $1,600	3		
4 Enter here and on line 12a, the amount on line 2, or line 3 if you elect the farm optional method	4		

[1] *Gross profits from farming are the total gross profits from Schedule F, line 28 (cash method), or line 70 (accrual method), plus the distributive share of gross profits from farm partnerships (Schedule K–1 (Form 1065), line 14) as explained in instructions for Schedule SE.*

Part II — Computation of Net Earnings from NONFARM Self-Employment

REGULAR METHOD 5 Net profit or (loss) from: a Schedule C, line 21. (Enter combined amount if more than one business.)	5a	-529	99
b Partnerships, joint ventures, etc. (other than farming)	5b	0	00
c Service as a minister, member of a religious order, or a Christian Science practitioner. (Include rental value of parsonage or rental allowance furnished.) If you filed Form 4361, check here ▶ ☐ and enter zero on this line	5c	0	00
d Service with a foreign government or international organization	5d	0	00
e Other (See Form 1040 instructions for line 36.) Specify ▶	5e	0	00
6 Total (add lines 5a through e)	6	-529	99
7 Enter adjustments if any (attach statement)	7	0	00
8 Adjusted net earnings or (loss) from nonfarm self-employment (line 6, as adjusted by line 7)	8	-529	99

If line 8 is $1,600 or more **OR** if you do not elect to use the Nonfarm Optional Method, omit lines 9 through 11 and enter amount from line 8 on line 12b, Part III.

Note: *You may use the nonfarm optional method (line 9 through line 11) only if line 8 is less than $1,600 and less than two-thirds of your gross nonfarm profits,[2] and you had actual net earnings from self-employment of $400 or more for at least 2 of the 3 following years: 1973, 1974, and 1975. The nonfarm optional method can only be used for 5 taxable years.*

SE

NONFARM OPTIONAL METHOD

9 a Maximum amount reportable, under both optional methods combined (farm and nonfarm)	9a	$1,600	00
b Enter amount from line 3. (If you did not elect to use the farm optional method, enter zero)	9b	DOES NOT APPLY	
c Balance (subtract line 9b from line 9a)	9c		
10 Enter two-thirds of gross nonfarm profits[2] or $1,600, whichever is smaller	10		
11 Enter here and on line 12b, the amount on line 9c or line 10, whichever is smaller	11		

[2] *Gross profits from nonfarm business are the total of the gross profits from Schedule C, line 3, plus the distributive share of gross profits from nonfarm partnerships (Schedule K–1 (Form 1065), line 14) as explained in instructions for Schedule SE. Also, include gross profits from services reported on line 5c, d, and e, as adjusted by line 7.*

Part III — Computation of Social Security Self-Employment Tax

12 Net earnings or (loss): a From farming (from line 4)	12a	0	00
b From nonfarm (from line 8, or line 11 if you elect to use the Nonfarm Optional Method)	12b	-529	99
13 Total net earnings or (loss) from self-employment reported on line 12. **(If line 13 is less than $400, you are not subject to self-employment tax. Do not fill in rest of schedule.)**	13	-529	99
14 The largest amount of combined wages and self-employment earnings subject to social security or railroad retirement taxes for 1976 is	14	$15,300	00
15 a Total "FICA" wages and "RRTA" compensation (15a)			
b Unreported tips subject to FICA tax from Form 4137, line 9 or to RRTA (15b)			
c Total of lines 15a and b	15c		
16 Balance (subtract line 15c from line 14)	16		
17 Self-employment income—line 13 or 16, whichever is smaller	17		
18 Self-employment tax. (If line 17 is $15,300.00, enter $1,208.70; if less, multiply the amount on line 17 by .079.) Enter here and on Form 1040, line 58	18		

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Figure 3: Schedule SE, "Computation of Social Security Self-Employment Tax."

Then when the point is reached at which taxable income is emerging, it is possible to convert fairly painlessly to the more detailed documentation that is desirable to support tax forms. It is important, however, to start keeping records of some sort immediately. Paper bags work well for some people, a simple spiral notebook for others (there are perhaps as many systems as there are people), but without records, no tax losses can be claimed, no business expenses can be substantiated, and no firm idea of the enterprises's success or failure can be developed.

Auditory Nerves

Any tax form is regarded as potentially fraudulent and, if it comes up for review, it is winnowed for *any* defect. (I have been reviewed in the past and it resulted in my receiving a larger refund.) New small businesses are especially subject to review, so extreme care is necessary when documenting expenses; but that care can pay off as a handsome tax loss or a watertight set of forms with which even the most eagle eyed taxman can find no fault. If you operate on the principle that you must be able to prove the legitimacy of anything you claim, you need have no fear.

Conclusion

If you're trying to make some money with your home system, why not start recording what the enterprise is costing you and what you're earning from it? You may be a small business already and you may be able to derive tax benefits from that status. Almost more important, wouldn't it be nice to know whether or not your enterprise is profitable? Give it a try, and before long you'll find that the additional tax forms hold no terrors for you.■

USEFUL GOVERNMENT PUBLICATIONS
Available from the Internal Revenue Service (free, on request)

Tax Guide for Small Business — publication 334
Recordkeeping for a Small Business — publication 583
Tax Information on Depreciation — publication 534
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The Motorola 6800 Instruction Set

Two Programming Points of View

Paul M Jessop
1157 Warwick Rd
Solihull
West Midlands B91 3HQ
ENGLAND

Instruction Field Encoding.

```
| 1 | X | X | X |   |   |   |   |   Group 1: Dual operand instructions
  0 = A, S   00 = I      OP
  1 = B, X   01 = D
             10 = X
             11 = E

| 0 | 1 | X | X |   |   |   |   |   Group 2: Single operand instructions
             00 = I      OP
             01 = D
             10 = X
             11 = E

| 0 | 0 | 0 | 0 | 0 |   |   |   |   Group 3: TPA, TAP and NOP
                          OP

| 0 | 0 | 0 | 0 | 1 |   |   |   |   Group 4: Condition code instructions
                          OP

| 0 | 0 | 0 | 1 |   |   |   |   |   Group 5: Accumulator instructions
                          OP

| 0 | 0 | 1 | 0 |   |   |   |   |   Group 6: Branches
                     Condition

| 0 | 0 | 1 | 1 | 0 |   |   |   |   Group 7: Stack and index register control
                          OP

| 0 | 0 | 1 | 1 | 1 |   |   |   |   Group 8: Interrupt and subroutine control
                          OP
```

Figure 1: One way to organize one's viewpoint of the Motorola 6800 instruction set is to view it as a number of instruction groupings, broken down by internal binary fields for selection of instructions within the group. This viewpoint is most appropriate for those working directly in binary, or organizing the code generation parts of an assembler or compiler.

When faced with the problem of trying to hand assemble a machine language program, the task of looking up each of the op codes in the manufacturer's data can be quite daunting. Admittedly, some become familiar before very long but the less common instructions still cause problems (do you 6800 users remember the hexadecimal op code for TPA?). Two solutions to this dilemma are suggested here. The first is suitable for "switch flippers" and the second for users of MIKBUG and other systems with hexadecimal dump and load functions.

The First Solution: Use Instruction Fields

Anyone who has seen the programming books for the DEC PDP 8 will be familiar with the principles involved. In the PDP 8 instruction set, the first three bits of the 12 bit word define the type of instruction and the remaining bits each have a separate function. This is of course a gross simplification and is not true for memory reference and IO instructions but it underlines the basic ideas. Now, study of the 6800 op codes reveals some interesting facts at the bit level. These are outlined in figure 1.

These patterns are naturally related to the instruction decoding which goes on inside the chip, but they are a godsend to the programmer who must work in binary. A couple of words of explanation are needed. Branch to subroutine occurs in an unexpected place but it is easy to remember if thought of as Jump, mode immediate. The generalization in group 1 bit 6 that a zero implies accumulator or stack pointer addressing does not hold true for compare index register (CPX), where it implies index register addressing. Naturally, the store instructions (STA, STS and STX) do not exist in immediate mode in the published definition of the 6800 instruction set.

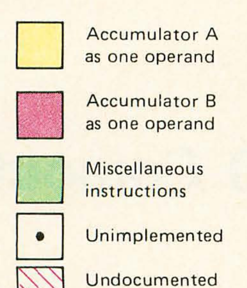
The Second Solution: The Ordered Manual Lookup Table

The appropriate information is contained in figure 2. This should be a great boon to anyone who, for lack of memory or IO

devices, has no assembler. The table is arranged in such a way that the first hexadecimal digit is the horizontal coordinate, just as the x component comes first in a pair of Cartesian coordinates. The credit for inspiring this technique must go to Mr Fugitt (March 77 BYTE, page 36) for his 6502 table, but this table for the 6800 is somewhat more useful for both assembling and disassembling because of the way the codes fall into groups and the addressing modes fall into neat vertical lines.

By way of a final word, the table can, if reduced small enough, make a very handy reference card. Mine has, on the front, tables to convert between hexadecimal, octal and decimal, and, on the reverse, the conditions required for branches, the restart vectors, details of the control code register and the stack register. ■

The Ordered Manual Lookup Table



NBA = And accumulators
HCF = Halt and catch fire
STS, STX, STA, STB = store immediates

See "Undocumented 6800 Instructions" by Gerry Wheeler, page 46, December 1977 BYTE.

Low (Second) Nybble					ACCA	ACCB	X	E	I	D	X	E	I	D	X	E
F	SEI	•	BLE	SWI	CLR	CLR	CLR	CLR	STS	STS	STS	STS	STX	STX	STX	STX
E	CLI	•	BGT	WAI	•	•	JMP	JMP	LDS	LDS	LDS	LDS	LDX	LDX	LDX	LDX
D	SEC	•	BLT	•	TST	TST	TST	TST	BSR	HCF	JSR	JSR	•	HCF	•	•
C	CLC	•	BGE	•	INC	INC	INC	INC	CPX	CPX	CPX	CPX	•	•	•	•
B	SEV	ABA	BMI	RTI	•	•	•	•	ADD	ADD	ADD	ADD	ADD	ADD	ADD	ADD
A	CLV	•	BPL	•	DEC	DEC	DEC	DEC	ORA	ORA	ORA	ORA	ORA	ORA	ORA	ORA
9	DEX	DAA	BVS	RTS	ROL	ROL	ROL	ROL	ADC	ADC	ADC	ADC	ADC	ADC	ADC	ADC
8	INX	•	BVC	•	ASL	ASL	ASL	ASL	EOR	EOR	EOR	EOR	EOR	EOR	EOR	EOR
7	TPA	TBA	BEQ	PSH B	ASR	ASR	ASR	ASR	STA	STA	STA	STA	STA	STA	STA	STA
6	TAP	TAB	BNE	PSH A	ROR	ROR	ROR	ROR	LDA	LDA	LDA	LDA	LDA	LDA	LDA	LDA
5	•	•	BCS	TXS	•	•	•	•	BIT	BIT	BIT	BIT	BIT	BIT	BIT	BIT
4	•	NBA	BCC	DES	LSR	LSR	LSR	LSR	AND	AND	AND	AND	AND	AND	AND	AND
3	•	•	BLS	PUL B	COM	COM	COM	COM	•	•	•	•	•	•	•	•
2	•	•	BHI	PUL A	•	•	•	•	SBC	SBC	SBC	SBC	SBC	SBC	SBC	SBC
1	NOP	CBA	•	INS	•	•	•	•	CMP	CMP	CMP	CMP	CMP	CMP	CMP	CMP
0	•	SBA	BRA	TSX	NEG	NEG	NEG	NEG	SUB	SUB	SUB	SUB	SUB	SUB	SUB	SUB
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F

High (First) Nybble

Figure 2: A second way of viewing the 6800 instruction set is from the viewpoint of a hexadecimal matrix. Here a map of the 6800 instruction set has been broken up into several overall regions, with color coding indicating references to accumulators A and B. Unimplemented and undocumented instructions are shown with a black dot; undocumented, but implemented instructions are shown with cross hatching to indicate "use at own risk."



About the Author

Bob Bumpous is a machine controls design engineer with Adolph Coors Company and has been doing discrete and computerized machine control design for the past four years. He previously worked for Bendix Navigation & Control Division on documentation of SKYLAB experiments. He is a 1969 graduate of Texas Technological College with a BS in engineering physics, and has an avocational interest in personal computing.

A User's Reaction to the SOL-10 Computer

Robert Bumpous
212 N Ford
Golden CO 80401

When I first saw the Processor Technology SOL it was love at first sight. After acquiring the SOL system, I found that it has everything (almost) a hobbyist needs in one package.

The SOL-10 system which I purchased consists of a single 10 inch by 16 inch board computer, a keyboard, a power supply and cabinet. Figure 1 shows a memory map of the system which gives an idea of its overall structure. Processor Technology also makes the SOL-20 which has a heavier duty power supply and backplane for five extra S-100 cards.

MEMORY MAP

Region	Address
PROGRAMMABLE MEMORY OR PROM MEMORY (USER SUPPLIED) 0000 - BFFF	0000
ROM OR PROM OPERATING SYSTEM	C000
1K USER MEMORY C800-CBFF (PROGRAMMABLE)	C800
1K RAM VIDEO DISPLAY CC00-CFFF	CC00
USER SUPPLIED D000 - FFFF MEMORY OR IO	CFFF
	FFFF

Figure 1: Memory allocations of the SOL design. Within the IO area at D000 to FFFF, the SOL-10 has a UART dedicated to the tape interface, a UART dedicated to the serial communications interface, a parallel keyboard interface, one 8 bit input port and one 8 bit output port.

The SOL single board computer is a complete beginning system. The board contains an 8080A processor with fully buffered data and address buses which are brought to a connector at the center of the board where an S-100 compatible backplane daughter board can be plugged in. It also has a complement of IO ports. The board and operating system are oriented around the parallel keyboard input port and video display output port. 1 K of the 2 K of programmable memory on the board is used to store the 64 character by 16 line video display contents. The output of the display driver is an EIA composite video signal (1.0 to 2.5 V peak to peak) which will drive any standard monitor or even a modified TV set. The full 128 upper and lower case ASCII character set is available for display. With the addition of a video monitor the system becomes a smart video terminal with either full or half duplex communications modes selectable from the keyboard.

The SOL design has an asychronous serial interface port with switch selectable data rates from 70 to 9600 bps. This serial IO port has both an RS-232 and 20 mA current loop output. Also included is an 8 bit

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Now obviously, we had to do a few things to bring the price down. The Model 20 has a somewhat shorter manual. Technically, it's not quite as complex. Don't kid yourself though, the Model 20 does a real job. You can control your computer to do such tasks as data entry, quality control and everything else where you want a "hands-off" operation. Elsewhere in the ad we've illustrated some examples of the kinds of things you can do.

About the Model 20

Heuristics' new Model 20 handles up to 32 words. Software is ROM based. The Model 20 uses 64 bytes per spoken word which is callable from BASIC.

Hardware includes 2 band pass filters with 2 bit amplitude, 2 zero crossing detectors and a linear amplifier.

The combined hardware/software/lab manual includes 10 experiments.

The ROM based speech recognition program occupies 2K bytes of ROM.

The Model 50, still a great buy at $299.

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Software includes SpeechBasic BASIC programming language in source and paper tape, assembly language speech recognition program in source and paper tape, hardware and self-test program in source and paper tape. SpeechBasic plot, correlation, recognition and advanced recognition programs are offered in source.

The assembly language program uses less than 4K bytes for a 32 word vocabulary. It loads at 100H. A high core version is available. SpeechBasic BASIC interpreter loads at 0 and requires 8K. A diagnostic program is included.

Documentation includes a 275 page lab manual with 35 experiments and a 100 page hardware manual. All manuals are now available as separate items. The big manual is ideal for schools and colleges as an introduction to speech and pattern recognition.

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Model 50 lab manual	$ 25
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(both manuals $35)	
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For more information visit your nearest computer store. Most dealers now carry the Heuristics line. Or if more convenient write for literature. Please address Heuristics, Inc., Box B, 900 N. San Antonio Road, Los Altos, CA 94022. Phone (415) 948-2542.



Circle 49 on inquiry card.

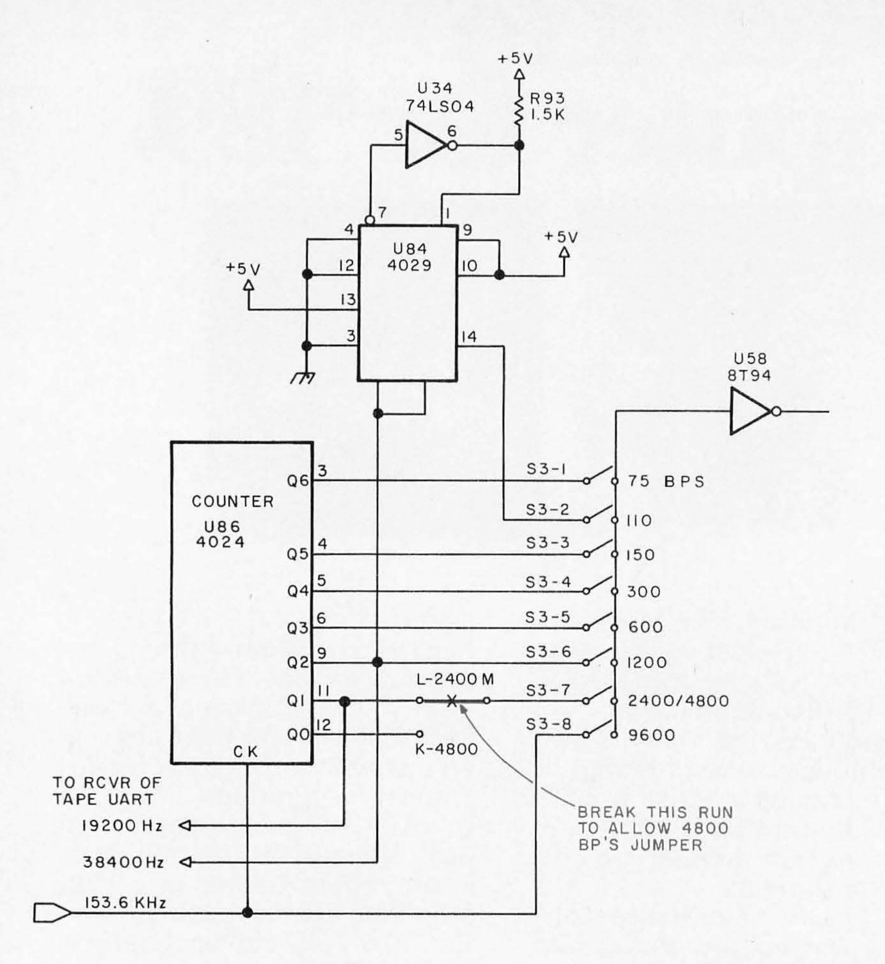


Figure 2: One minor printed circuit bug found by the author in testing out the SOL computer was the run from point L to point M from U86 to the data rate selection switch. If 4800 bps operation is desired as an option, the run in question has to be broken and a jumper wire from point K to point M on the board has to be substituted.

parallel IO port which allows a user to drive any external peripheral.

An option which I think is important to any system is the cassette interface. This option, used with the SOL, allows the user to read or write programs or data to a cassette tape at a software selectable rate of 300 bps or 1200 bps using standard asychronous Manchester coded signal at 1200/2400 Hz or 600/1200 Hz.

The SOL-PC board itself is a high quality double sided G-10 type material with plated thru holes. There is an excellent solder mask on the board with all component locations clearly labeled. The unit I received, which was Revision D of the board, had two defects which Processor Technology asked the assembler to change: two lines crossed on the same side of the board and two lines to the S-100 bus were reversed. Both were easy to correct and I'm sure these defects will have been corrected on the next revision of the board.

I also discovered what I think is another error on the board. In the circuit that selects the serial data rate there is a jumper that enables either 2400 or 4800 bps to be switch selectable. The board had the switch permanently connected to the 2400 bps position. This caused the serial IO to work improperly when 4800 bps was selected. Because there are lines feeding from this circuit to the cassette interface circuit, the cassette interface would not work properly. The problem is easily corrected by breaking the lines between the L and M jumper contacts (see figure 2).

There is a moderate amount of large scale integration on the board. The 8080A processor, the ASCII 7 by 9 dot matrix encoder, the two UARTs used for the serial and cassette tape interfaces and the 5204 (512 by 8) EROMs in the personality module are the LSI chips used. The programmable memory for the computer and display is made up of 2102 parts. All of the IO select switches and the IO connectors are located at the rear of the board for easy access. The personality module is located along the back edge to allow an easy change of the operating system.

The system timing is derived from a 14.31818 MHz crystal controlled oscillator that feeds the video character generator, UARTs, and 8080 clock divider circuits, MSI and SSI TTL along with an AH 0026 dual MOS clock driver supply the 8080 clock signals. There is an RC charge-up circuit that provides an automatic reset signal when power is turned on and a controlled "wait" period immediately after the reset signal.

The keyboard supplied as part of the SOL-10 system is a custom unit from Key Tronics which connects to the SOL-PC board through a ribbon cable connector which plugs into a header on the board. The keyboard uses no LSI encoder and no mechanical contacts and can easily be disassembled for cleaning.

The keyboard is easy to assemble and check out. All of the data bits are latched so that they can be examined at leisure. The strobe bit is only on for a very short time, two to ten μs. There is only one tricky part of the keyboard assembly procedure. This is the installation of the four SIP resistor networks. Extra care must be used in installing these since they are not as clearly marked as most of the other items, and the two different sets of values will not allow the keyboard to work properly if interchanged.

The power supply for the SOL-10 consists of a power transformer, an external filter capacitor for the 5 V supply and a regulator card to supply the required vol-

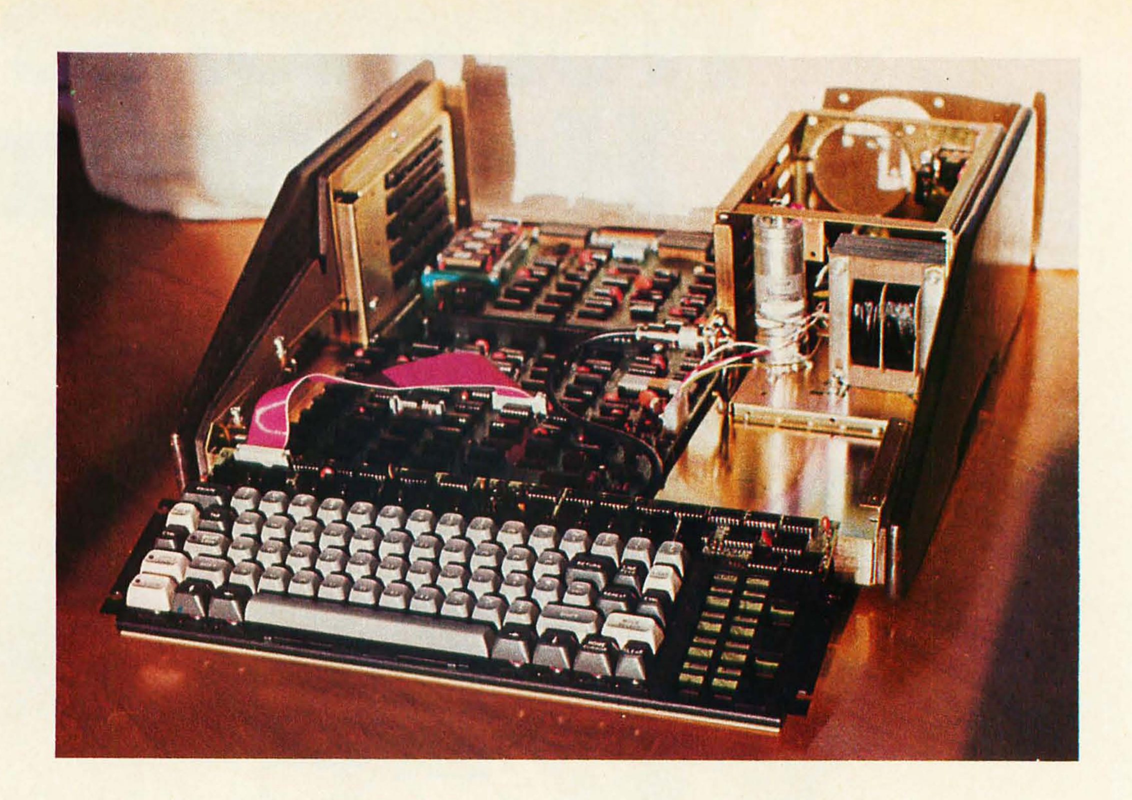


Photo 1: Processor Technology SOL, with cabinet cover removed to reveal its inner secrets.

tages (12 VDC at 150 mA, 5 VDC at 2.5 A, -12 VDC at 200 mA) to the SOL-PC and keyboard. The SOL-20 system power supply, in addition to these voltages, provides 16 VDC at 1 A unregulated, -16 VDC at 1 A unregulated, and 8 VDC at 6 A unregulated for the backplane Altair (S-100) bus daughter board. The regulated 5 V to the SOL-PC board has an over voltage crowbar on its output which, on my original version, had an overly sensitive turn on characteristic. Processor Technology has since sent a revision which corrected this problem.

The SOL system cabinet is sheet metal with solid walnut sides. It is designed to house the SOL-PC, the keyboard, power supply, backplane and five additional S-100 cards in a fan cooled card cage. The cabinet is constructed so that the power supply is isolated from any radio frequency interference (RFI) switching transients in the memory or processor cards. The whole system looks well shielded, which is an important consideration in this age of CBers. The walnut sides come sanded but unfinished; they look nice but take a lot of time to finish properly.

The assembly manual that came with the system describes the assembly procedure very well. It features the kind of complete, step by step format that kit builders have come to expect. It seems very complete, including pictures and drawings of how to assemble the components and subassemblies into a useful computer and terminal. However, there were no flowcharts, block diagrams or explanations of how the different sections of the computer are supposed to work, or how they interact with each other. As of this writing (spring 1977) I have still not received two sections of my manual, operating procedures, and theory of operation. Most of the information that I have on the operation of the machine has come from an article in the February *Digital Design* by Lee Felsenstein of LGC Engineering and Robert Marsh (vice president of Processor Technology), who are the codevelopers of the SOL terminal system. This article gives a fairly complete though not detailed description of the operation and interactions of the SOL system components.

The CONSOL operating system, which is the minimal operating system, is stored in 1024 K bytes of EROM starting at C000. This operating system has seven commands that can be executed from the keyboard, sufficient to allow the operator to enter his or her own programs or prerecorded programs and execute them. The following are the commands available through CONSOL:

1. DUmp ADDR1 ADDR2 dumps the contents of memory between address 1 and address 2 onto the CRT terminal in a hexadecimal format.
2. ENter ADDR1 enters hexadecimal format data into memory starting at address 1.

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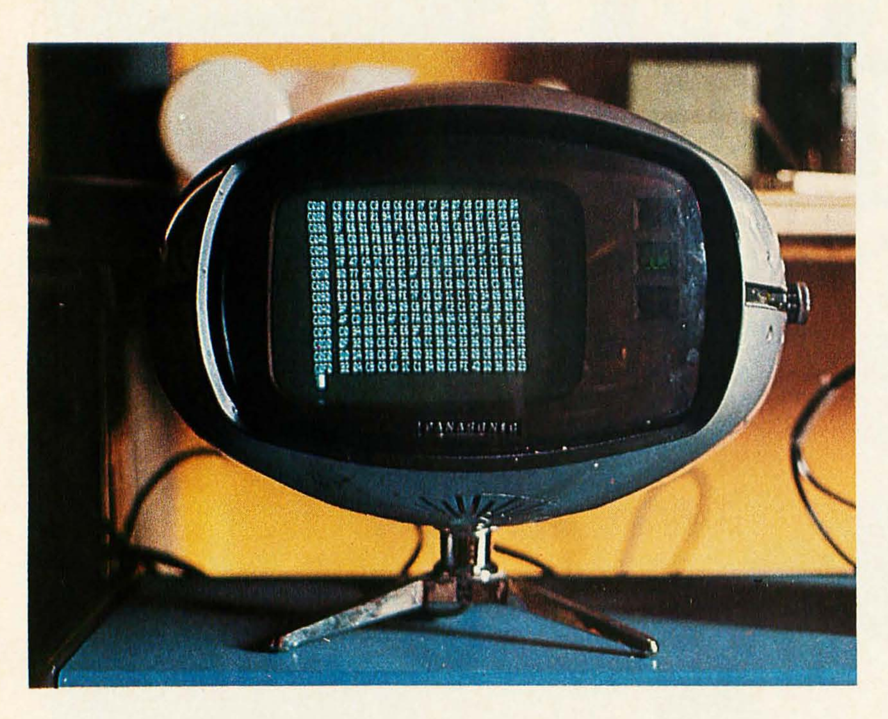


Photo 2: The SOL's display generator produced this video character graphics pattern on the author's television monitor.

3. EXecute ADDR1 executes a program in memory starting at address 1.
4. TErminal is a program designed to allow the SOL system to be used like a standard CRT terminal with serial 20 mA or RS232 interface. This ability could make the SOL system very attractive to a small business user who needs an inexpensive terminal.
5. TL (tape load) loads a prerecorded cassette tape into memory at an address specified by the tape. The information supplied with the software doesn't give a very good definition of how the TL command looks at the tape header data. Because of this, it is very difficult for the user to configure a tape-header for any data he or she would like to store on a cassette.
6. BAsic executes a program located at address 0000, typically BASIC.
7. The final command is the MODE command which calls a program that allows all the other commands to be entered on the keyboard and recognized by the computer system.

The early version of CONSOL which I received does not have a command to dump data from memory into a cassette tape. This is a great disadvantage when trying to develop a program. Whether the program being developed bombs out or is successful, it is nice to have a copy so it doesn't all have to be typed in again.

The purchaser of a SOL system is also supposed to receive a 5 K BASIC operating system with the purchase of the on board audio cassette interface. This 5 K BASIC includes two computer video games. I had not yet received this when this article was written in the spring of 1977.

I ordered my SOL system on September 4 1976 and anxiously awaited its arrival. Only a portion, the SOL-PC, arrived on November 18 1976 along with part of the manual. When I opened the box I was confronted with what appeared to be a rather large, random accumulation of parts. However, all of the parts called out in the parts list were there. The assembly would have gone faster if the components had been sorted, placed in small bags, and marked as to the section of the assembly procedure they were for.

The procedure given in the manual calls for construction and checkout to proceed together. To follow the manual you must have a power supply and keyboard to properly assemble the complete SOL system. Because I didn't have either of these items, I was only able to proceed with the assembly until I came to the first step, which required the power supply; there I stalled. I spent all of Christmas 1976 lurking around the mail box, awaiting the delivery of the rest of my system. Finally, on January 4, it arrived and off to my basement "laboratory" I scurried, not to emerge "til the beaste was up and running."

After much soldering, bending and clipping, I reached the point of the first operations test. I plugged in my TV monitor, turned on the SOL system power, hit the MODE key, and typed in the DUMP command. Nothing! All I could get was the CURSOR in the upper left hand corner of the screen. This is when the lack of block diagrams and explanations of the system really hit me. After what seemed an extremely long time, I managed to solve the problem. The display uses the first several words of user memory to store the line and character positions for the video display, and somehow, in my haste to complete the assembly, I had bent a pin under on one of the memory chips. Dumb, but almost impossible to locate. Once this problem was solved, the rest of the system went together very smoothly.

The total assembly time, excluding the

time I spent looking for my own error, was about 36 hours. The sanding and coating of the walnut cabinet sides took about five more hours. I used clear satin polyurethane finish of the type found in most hardware stores. This is a very hard, clear, fast drying resin that puts a tough, mar resistant sealer on the side panels.

Overall, I feel that the Processor Technology entry in the microprocessor race is a good buy. I have had what seems to me excessive delays but I believe that now that the production of these units is in full swing, there should be a minimal amount of lead time on the system hardware. Processor Technology says that they have sold almost 1,000 of these systems. The software development, however, seems to be lagging well behind the hardware as might be expected from the history of computer science in general.

If you are planning to develop your own software or plan on buying it somewhere other than Processor Technology, the SOL system will serve you nicely. The CONSOL routine provides a step up from the front panel toggle switch design philosophy of most of the other microcomputer manufacturers and I feel it warrants the purchase of this system.■

Editors' Note:

At the time this article was edited (August 15 1977) a SOL-20 with 16 K memory and CONSOL was resident in our office at BYTE. 5 K BASIC is now being delivered, according to Terry Holmes of Processor Technology.

The Following Comments Were Received from Bob Bumpous with His Author's Proofs on October 7 1977.

Since completing my SOL-10 I have written a couple of short programs to test the various hardware options of my system.

I have also purchased the SOL upgrade kit which adds the larger power supply fan and backplane and an IMS 8 K memory.

I have received the two missing sections of my manual and my BASIC tape. I have not yet been able to run BASIC due to a problem I'm having getting my cassette tape interface to operate properly.

I have also received my SOLOS operating system; all of the functions except the tape interface seem to work well.

Walter Banks
Computer Communications Network Group
University of Waterloo
Waterloo, Ontario CANADA

The Waterloo RF Modulator

In recent months a number of projects have taken advantage of the special input characteristics of Schmitt trigger TTL parts. They have been used as oscillators, monostable multivibrators and signal conditioning elements. This reminds me of a simple circuit I used as a video radio frequency generator when I worked on a low cost terminal development project.

As can be seen from the schematic, IC1A is a conventional free running Schmitt trigger oscillator running at one third of the desired television channel carrier frequency. For example, channel 3 would require it to oscillate at about 20 MHz. IC1B acts as a buffer whose output is a square wave at the fundamental frequency of the oscillator. A square wave has odd order harmonics, the second of which is at three times the fundamental, the third at five times, and so on.

Q1 modulates the generated radio frequency output by varying the effective power supply voltage to IC1. Since standard video is one volt peak to peak, the modulation depth is about 20 percent in this circuit when using a standard 5 V supply.

Most low cost television sets have a hot chassis, therefore a simple capacitive connection is provided by connecting a 6 inch piece of 300 ohm twin lead to the output of IC1B and the computer's ground, and taping a second piece of 300 ohm twin lead to the top of the first making physical contact but not direct electrical contact. The second piece of twin lead is then connected to the set's antenna terminals.

As with all radio frequency devices, normal caution should be exercised with this device in preventing unwanted interference. (For example, don't leave your antenna connected to the set if you want to keep peace with your neighbors.)■

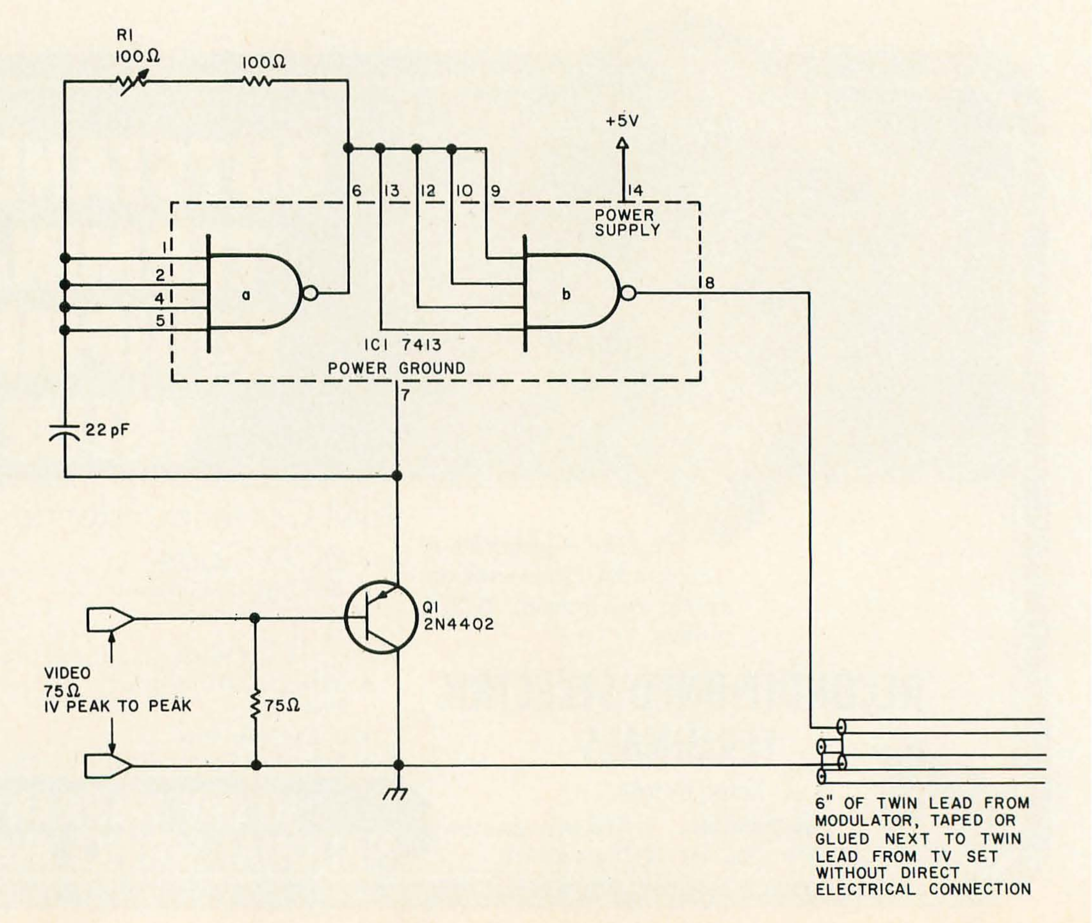


Figure 1: The Waterloo RF Video Modulator. This circuit works by modulating the power supply voltage of a digital integrated circuit. The frequency of oscillation is set by resistor R1 and should be adjusted for best reception on the chosen channel. Capacitive coupling between two DC isolated sections of ordinary twin lead gets the signal into the television set without any worries about AC ground problems.

MSD

What You See is What You Get!

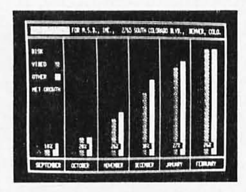
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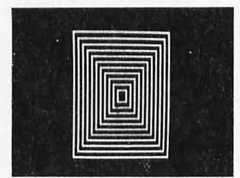
MSDV-100 Video Display System:

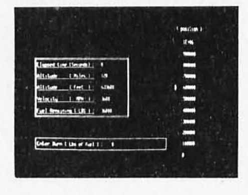
The Video Display System is a high quality 80 character, 24 line video output device for the S-100 bus. Many advanced features have been incorporated which are not normally found on units costing many times the price.

The character set includes upper and lower case characters as well as full punctuation. Any character can be underlined, a feature useful in word processing. A character can also be made to blink at a user selectable rate, often used for alarm or warning situations. Additionally a character can appear in reverse field (black on white) or, if composite video is used, individual characters can be intensified.

Also included in the MSDV-100 is the ability to generate high quality continuous forms overlays. Charts, graphs, or order entry forms are easy to produce on the video screen.







A third significant feature of the Video Display System is the ability to display grey scale elements in any of nine levels in any of 1920 positions on the screen. This is especially useful for bar graphs and for grey scale graphics or animations.

Internally, the MSDV-100 is a two-board S-100 based system which occupies 2K of RAM address space and two I/O ports, user selectable. The microcomputer can write to the screen directly with horizontal retrace synchronization if desired for a flicker free, very high speed display.

Software support for the MSDV-100 is complete with both machine language code, including fully commented source listings, and a comprehensive Basic software package implementing all MSDV-100 features. Assembly language drivers allow the sophisticated user to easily customize the system for specilized applications.

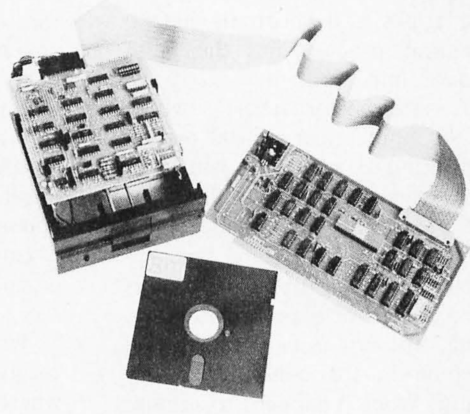
Programs are provided that permit the user to link the video system to high level programming languages such as Basic. A link program, provided in Basic, permits the user with no knowledge of assembly language programming to immediately obtain video output. The link fully implements the forms capability of the MSDV-100, including direct cursor addressing, as well as the other advanced features of the Video Display System.

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The disc controller design is totally synchronous, requiring no "one shots". Ease of maintenance is evidenced by the fact that there are no adjustments required for operation.



The Altair/S100 compatible disc controller is a single board design, and features very low power consumption.

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sense organs, and the design and execution of movements in space, lend themselves perfectly to parallel processing in small subunits. Here the brain can vastly outperform our typical current computers which have only one, or at most a few, processing units capable of simultaneous operation. For example, all of the data in the visual field is available simultaneously on the surface of the retina. Rather than dealing with it point by point, the brain sucks it all in at once in one enormous byte and sets to work on the analysis of many small areas of the visual field simultaneously. (We shall examine its algorithms in detail later.)

Even with the small cheap processors available to us now, we could obviously never afford to match the brain in quantity. However, we don't have to go to the other extreme and try to do it point by point serially with a single very fast processor as has been typically attempted. The job is just too large for even the fastest machine to do this way, and there are certain advantages as well in terms of the feature extraction process to having a basically parallel system. On the other hand, we do have a speed advantage and it certainly should be possible to simulate the operation of a number of the brain's processors with only one of ours in the same time frame. (There will be some increase in complexity where the results of neighboring units are interactive.) Just how to optimize this sort of tradeoff is, of course, a matter for much study. A first step which we shall take here will be to examine some of the tricks and shortcuts in the feature extraction process that the brain itself uses to save time.

The third system characteristic which results from the brain's hierarchical organization is high survival value. We will learn nothing about Asimov's first two "laws" of robotics (the protection of human beings) by studying the brain. The third law, ensuring the survival of the robot, has always been a major concern of brain architecture. It is annoying, but not usually fatal when the big machine in the computer center develops a fault. When it happens to a brain, or in the situations we will send them into, a robot, the whole device may be destroyed. The redundancy inherent in the brain's basic structure is, of course, valuable in this regard, but there is more to it than that. Recall two facts about the brain: There is an evolutionary order of development to its structure, and the major functions have representation at all levels. These two facts are related. Whereas our computers have never been expected to incorporate pieces of earlier models, the brain in the present form contains most of the parts of its earlier forms. The simplest early brains obviously had to be capable, in their own inelegant way, of getting the organism around in the environment and surviving. During the course of evolution, more complex structures capable of more sophisticated handling of the same basic functions became available. Rather than eliminating the older structures and duplicating their functions, the newer ones simply took control of the older and used them as subprocessors. A fairly general principle of organization evolved in which the higher level structures control the lower not by turning them on when needed, but by inhibiting their actions except as desired. The beauty of this system is that if a higher center is suddenly damaged, the older, more primitive units which it normally holds in inhibition are released to function on their own. Thus, damage tends not to eliminate vital functions, but only to downgrade the complexity with which the job can be performed. This is especially true of functions such as defense. The typical result of damage to higher brain centers is a "nasty" animal, ie: one which can adequately fight, but which fails to make fine discriminations about the appropriate stimulus conditions for doing so, and which defaults in the safe direction by attacking any strong stimulus source. Of course this kind of thing has its limits, and this is particularly true of the most highly developed brains where some of this type of organization is sacrificed in order to give the highest centers direct access to the lowest for feedforward in the control of complex operations.

In the case of damage to lower centers, the multitude of processing elements available allows some of the higher levels to be reprogrammed to take over the functions of lower level systems by simulating their operation. The process takes a little time to organize, but it can be quite effective if the organism can survive for a few weeks while reorganization takes place.

While it is apparent that it is not possible to give a definite answer to the question of where a function of any complexity is performed in the brain, it may be useful (for orientation to the device) to identify some of the anatomical divisions of the brain shown in figures 3 and 4 with some of the functions which have important representation at those levels.

The lowest level of the central nervous system, the spinal cord, is a major route of input and output to the rest of the brain. With the exception of a few special cases, most of the sensory input from the body and most of the output to the muscles passes through this structure. Although it contains

immense fiber tracts, it should not be considered merely a cable. The nuclei of the spinal cord perform many important functions as intelligent terminals on both the input and output sides. Moreover, some simple actions are processed entirely at the level of the spinal cord from input to output. Everyone has seen an example of such a "spinal reflex" in the knee jerk produced by their doctor's rubber hammer.

The medulla and pons are also importantly involved in "intelligent terminal" types of IO activities, but at the so-called suprasegmental level of control. That is, these structures are frequently concerned with coordinating the activities of the IO routines in the cord so as to direct activities that involve the entire body rather than individual segments such as a single limb. For example, the pattern of motor activity involved in walking requires the coordination of the whole body to maintain balance as the center of gravity shifts, etc (such things as the decision to walk, and the choice of direction are in the province of higher centers). The medulla and pons also have important relations to a number of the special senses such as hearing and balance which are not represented throughout the body. Some of this sensory information is utilized immediately as input to supra-segmental reflexes, and some is processed for output to higher centers.

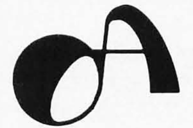
A complex physiological organism requires a great deal of regulation of its internal environment; the temperature must be exact, the heart rate must be regulated, inhalation must be controlled. These "housekeeping" routines also have representation at this level of the brain.

The mesencephalon is in many ways similar to the pons and medulla in its functions. In general, there is a transition from higher to lower degrees of abstraction in these IO systems as one progresses from the mesencephalon down to the medulla. The mesencephalon is in addition one end of a system, originating in the limbic system of the forebrain, which is important in regulating the type and intensity of the high level processing performed by the more advanced structures of the forebrain. There are two systems of the brainstem (medulla, pons, and mesencephalon) which may be mentioned in this context. The first is a system known as the reticular formation which has important functions in the brain analogous to the vectored interrupt system of the computer. It continually monitors the input of all the sensory systems, more for quantity of activity than for detailed analysis, and controls the degree of activation of various portions of the higher centers on this basis. Thus, it can immediately arouse the brain when a novel or intense stimulus is encountered, and jump the whole system to a stage of attention to, and analysis of, the important event. It also seems to exercise similar functions on the output side of operations.

The second "system" of the brainstem might be called the "amine" system, because it consists of a set of interacting nuclei which use various compounds of the chemical class known as "amines" in their operation. This system has a great deal to do with the mode of operation of the rest of the brain. Like the reticular formation, with which its activities are integrated, it sends its axons into all parts of the brain to make synaptic contacts with large groups of neurons in the forebrain and the brainstem and cord. Since the axons of these few neurons make millions of synaptic connections with vast numbers of neurons, we might expect that their function was a regulatory bias rather than the transmission of very specific information, and this appears to be the case. These nuclei are involved in such functions as regulation of waking, sleeping, and dreaming states, and apparently other "altered states of consciousness" since the hallucinatory drugs such as LSD are thought to exert their major effects here. Problems in some of these amine systems appear to underlie such abnormal operational modes as schizophrenia. Some portions of the amine system also regulate the intensity and selection of the various detailed patterns of activity generated by higher structures. Thus, in Parkinson's disease, which involves a disorder of part of this system, the ability to execute voluntary activities is impaired, although the conception of them is not. The systems of the brainstem thus exert a very major control over the general types of activity in which the higher levels of the device engage. A very interesting development here is the closing of this loop by return projections from the highest levels of the brain, the cortex, which allows the machine to gain control over its own status. This loop is fundamental to the phenomenon of consciousness.

Lying above the pons is the structure known as the cerebellum. This device is a subprocessor for some types of motor output. It is basically involved in the parallel to serial conversion of output that is not to be continuously modified by feedback control to the higher levels which specify its input. It can accept a parallel byte which defines an action to be undertaken, modify it to incorporate the current status of many variables of limb position, loading, etc, and

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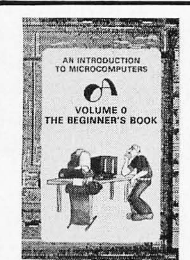


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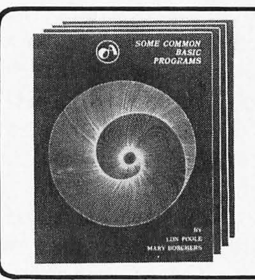
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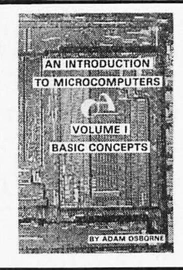
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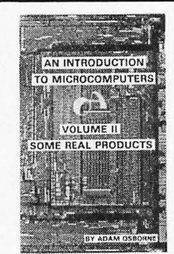
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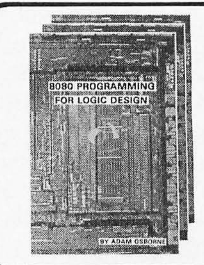
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convert the instruction to a series of sequenced operations with specified durations. Damage to the cerebellum has no effect on conscious processes, but seriously impairs the performance of muscular actions.

Above the mesencephalon, we encounter the diencephalon. The two major subdivisions, thalamus and hypothalamus, are quite different. The hypothalamus is heavily involved in the sort of housekeeping functions mentioned earlier. It controls the secretions of the endocrine system, for example, and is involved in a wide range of functions such as temperature regulation. In its role as chief executive of internal operations it, of course, must continually monitor internal conditions. These internal conditions in turn are frequently the ultimate sources of the whole brain's functional orientation. Thus, if the hypothalamus detects a low level of sugar in the blood, it initiates a state which we experience as hunger. This state represents a reorganization of the brain's systems for the control of goal directed behavior which causes the organism to engage in food seeking behavior. The hypothalamus thus contains part of the brain's analog of a computer's priority interrupt system. On the output side, the hypothalamus is important in changing the state of the internal body functions to correlate with higher priority interrupts. For example, if the limbic system initiates a "danger encountered" state, which we experience as fear, the hypothalamus must see to it that the body is mobilized for action with regard to blood flow, adrenaline levels, etc. The hypothalamus is also an important link in the limbic system-mesencephalon organization that in general specifies goals based on drives and emotional states for use in selection of overt behavioral activity.

The thalamus, the other major component of the diencephalon, functions as a very high level IO processor which prepares information for, and in part organizes the activity of, the cerebral cortex. Arrival of sensory input in the thalamus is sufficient for some rudimentary conscious experience of sensation, at least in some sensory modalities, but any very detailed resolution of the experience requires the enormous digital processing power of the cerebral cortex. In many respects, the various cortical areas act as subprocessors doing detail work for the various nuclei of the thalamus which route the information to and from them. Some thalamic-cortical systems are concerned with simple feature extraction of the input data, others with extrapolation of current events, and yet others with transmission of these extractions and extrapolations to other parts of the brain which, for example, evaluate them for relevance to current drive states or return sets of similar data from memory.

In this activity, the limbic system functions in the analysis of current and extrapolated data for relevance to the organism's needs. Thus, when we are hungry and see food, the limbic system in conjunction with the other structures mentioned earlier initiates a state which enables the sensory signal of food to initiate appropriate behavior, which is generated in detail by the cortex-thalamus-striatum apparatus. We experience the operation of this state of the limbic system as pleasure. If on the other hand, the limbic system recognized unfavorable situations, other states are generated (experienced as fear or anger) which cause other sorts of detailed actions to be generated.

The striatum, like the cerebellum, is importantly involved in the organization of motor output. It generates patterns of movement on the basis of input from analytic cortical areas, which are regulated in intensity by inputs from the amine systems under the direction of the limbic system, and it outputs these patterns both to the movement controlling areas of the cortex, and more directly to lower motor mechanisms. Unlike the cerebellum, the movements generated in the striatum are under continuous control of the cortex, and since the cortex is continually receiving and processing sensory information from the environment, a closed loop system is formed. This system is importantly involved in "voluntary" and learned movements.

We have already mentioned most of the functions of the cortex since it is of necessity involved in almost all the higher functions of the other brain structures. Its operation is essentially that of a vast decoding and encoding network which gives analytic and synthetic power to the operation of the other systems. Without it, their operation would be the same in type, but would be much reduced in capability due to the loss of capacity for fine distinctions and discriminations on the one hand, and large scale generalizations and synthesis on the other. The cortex first appears in other than rudimentary form with the evolutionary appearance of the mammals. Their behavioral diversity and plasticity as compared with the stereotyped, reflexive, instinctive behavior of the reptiles is probably associated with this structure.

This brings me to the final general point I want to make about the brain before we consider the detailed operation of some of its functions. One of the most important features of the brain is that it learns. Our

computers learn in a limited sense during programming, and some programs can learn to improve their performance on the basis of experience. This latter type of learning is characteristic of the way the brain operates, and it applies the process to almost everything it does.

You will notice that when I described some of the general functions of the different regions of the brain, I made no mention of memory. This is because we have no idea where it is. Indeed, the evidence suggests that the brain's memory is incorporated into its structure at whatever point the stored information is to act. Its memory then may be thought of as being distributed throughout its structure. At present, we can offer only speculation as to the physical nature and detailed processes of the brain's memory storage. Fortunately, we know a great deal about the operation of the brain's memory as a "black box" so that we can understand how it enters into the brain's algorithms, and we do not really need to understand its detailed physical nature to effectively use its principles of operation. Our current memory chips are a little inferior to the brain's memory in terms of capacity, but they are superior in speed and accuracy. Some programmable scratch memory and ROM chips associated with each of a robot's processing elements would do nicely, especially if supplemented by a disk for slow mass storage.

Researchers identify at least two types of learning that the brain permits, both very pragmatic. It has found that things that have occurred sequentially several times are likely to do so again, so it learns to associate them and act in anticipation. Thus, if the reflexive response of the nervous system to a painful stimulus applied to the foot is to quickly flex the leg, and if such a painful stimulus is repeatedly preceded by a "neutral" stimulus such as a bell sound, the brain will quickly learn to flex the leg whenever the bell sounds. This is the so-called "Pavlovian conditioned reflex." The potential utility of this scheme is obvious. Assuming the natural reaction to the painful stimulus is of use to the organism, then performing the reaction in response to the antecedent neutral stimulus allows the organism to get a jump on the world and perform more efficiently. This kind of action, although not the capacity to learn it, is employed in some computer memory systems which anticipate the next address call. Two limitations of this type of learning should be noted. The first is that the only thing that can be learned is the early performance of the natural response to the second stimulus. Thus, the organism's behavioral repertoire is not expanded, just made more efficient. The other is that all that is necessary for this type of learning is temporal contiguity of the events; it does not matter whether or not the anticipation is successful in improving the results. If you tape an electrode to the foot so that a shock following a bell occurs whether or not the leg flexes, the flexion of the leg still gets conditioned to the bell.

A second type of learning in which the brain engages is called "operant conditioning." This is the type of learning that permits us to expand our behavioral repertoire and base such expansions on the quality of the results. Simply stated, this type of learning is based on the principle that behaviors immediately preceding a reward are increased in future probability of occurrence. "Reward" here refers either to some pleasing event occurring, or some unpleasant state being terminated. Thus, behaviors that lead to good results will tend to recur. If we now add to this the second principle, that the behaviors immediately preceding the reward are the most strongly affected, it follows that more efficient behavioral routes to the reward are more strongly affected than less efficient ones. In this fashion, whole new behavioral patterns are built up out of successful components of more or less random exploratory behavior, and these quickly become welded together into tight and effective behavioral sequences.

The more developed brains rely very heavily on learning to produce most of their behavioral patterns. Less developed ones rely most heavily on prewired inflexible behaviors. Thus, evolutionarily primitive brains, such as those of fish, amphibians and reptiles, while capable of limited learning, generally rely on wired in behavior patterns that are available at birth. The advantage is early ability of the immature organism to fend for itself. The disadvantage is inflexible behavior that cannot easily adapt to an environment that differs from that in which the species evolved. Advanced mammals on the other hand, particularly man, are characterized by heavy reliance on learned behavior, which results in a protracted state of infantile helplessness followed by enormous behavioral flexibility and adaptiveness.

The parallel with our current attempts at robots is obvious. The major hurdle is designing a system that can operate in a generalized environment rather than being restricted to a specialized one with which it is preprogrammed to deal. The answer is also obvious. A successful robot must be capable of operant conditioning including the ability to be rewarded for successful at-

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tempts and to feel punished otherwise. This device is carried to such an extreme in advanced brains that even our basic ability to see, our perceptual structure, is learned in infancy. A newborn child has only the most rudimentary ability to interpret its visual environment; the relation between movement of the limbs and the result in visual space, the relation between certain output commands and the result on auditory input, all this and much more is painfully learned by trial and error in advanced brains. The result is the ability to modify behavior towards desired ends rather than react to stimuli in a preprogrammed fashion. The apparently random play of infants is in fact a deadly serious matter. Its emulation in our machines will be of the utmost importance to their handling of the generalized environment.

From this overview of the brain and its functional organization, it is apparent that we must now select a limited set of brain functions to discuss in detail. I think that those of most practical interest to robot designers at the present time are:

1. The brain's mechanisms of output control, including coordination and timing, and the use of feedback in the design and execution of movements in space.
2. The brain's mechanisms of sensory perception, including its principles of feature extraction, and the tricks and shortcuts that it employs in pattern recognition.
3. The brain's mechanisms for achieving goal-directed behavior, including mechanisms of emotion and motivation and their control of behavior patterns.
4. The brain's mechanisms of consciousness, intelligence and learning.

I will attempt to cover each of these subjects in some detail in this series of articles. Next month the series continues with a discussion of the output generations of biological computing devices.■

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Where KAISSA Founders on a Bug and CHESS 4.6 Conquers All

The Second World Computer Chess Championships

About the Author

Peter Jennings is author of MICROCHESS, a 6502 chess playing program developed for the KIM-1, and seen in operation at the PC 77 show in Atlantic City NJ. MICROCHESS 1.5 versus DARK HORSE is a match that Peter expects to report upon in the near future to give personal computer users an idea about the prospects of entering small systems in international chess competition.

Peter R Jennings
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Toronto, Ontario
CANADA

The Second World Computer Chess Championships were held on August 7, 8, and 9 1977 at the Hotel Toronto in downtown Toronto Canada under the sponsorship of the International Federation for Information Processing (IFIP). 16 programs from the United States, Canada, USSR, United Kingdom, Switzerland, Netherlands, West Germany and Sweden competed in a 4 round Swiss style tournament for the world title.

The event drew large audiences of spectators including computer and chess experts from around the world. In attendance was Mikhail Botvinnik from the Soviet Union, world human chess champion during the period from 1948 to 1963. Also attending the event was Hans Berliner, former world correspondence chess champion and author of J Biit, an earlier chess playing program. Lively expert commentary was provided by international master and computer chess author, David Levy, who is watching computer chess developments very closely these days because his wager of 1968 that no computer chess program will beat him in a tournament before August 1978 is about to run out.

The trend evidenced by the competing programs seems to be toward larger programs running on faster machines. Three of the programs ran on Amdahl 470/V6 computers, and CHESS 4.6 was running on CDC's Cyber 176. At the other end of the spectrum, OSTRICH was the only program running on a computer at the tournament site. A Data General Supernova was used. Communications were provided to remote data centers as distant as England, Germany, and California for the nonportable programs.

The 16 entrants were initially ranked on the basis of previous play before the tournament. In the first round, the eight superior programs were played against the

CHESS 4.6

For the next three years CHESS 4.6 will be the reigning world champion computer chess program. CHESS 4.6 was written in the CDC assembly language by David Slate and Larry Atkin at Northwestern University in Illinois, and runs on the CDC Cyber 176 located at Arden Hills MN. Initial work on the program began in the spring of 1968 and revisions have followed almost continuously since that time. Different versions of the program have held the US Computer Chess Championship title in 1970, 1971, 1972, 1973 and 1975. The program placed second in 1974, and second at the First World Computer Chess Championships, also that year.

CHESS 4.6, like almost all chess programs, plays chess by generating the possible legal moves for each side and evaluating the resultant position. The evaluation of this resultant position usually requires the generation of subsequent moves until a value can be ascertained, or until the time allotted to the evaluation has expired. Because of the number of moves normally available in a chess position (average 42), the number of terminal positions which must be evaluated grows exponentially with the depth of the search. Many programs restrict the number of moves they examine as a means to extend the depth of search. CHESS 4.6, on the other hand, conducts a full width search but is consequently restricted in the maximum depth to which it can evaluate a position. It must also evaluate each terminal position as rapidly as possible.

The evaluation of each position is based upon the material and positional factors. The material factor is considered to be the most important as most chess players will agree. The positional factor is limited in importance to less than the value of 1½ pawns in material difference. The value of any given position is based on the material difference between the sides and on penalty and bonus points allocated for positional factors such as: the pieces under attack, the pawn structure (doubled, isolated, passed or backward pawns), the rock positions (squares controlled, enemy king tropism, doubling, file control and seventh rank), the bishop position (square control and development), the knights (king and center tropism, and development), the queen position (square control and king tropism) and the king position (safety, center and pawn tropism). Two different algorithms are used: one for positions involving an even material position, and a "mop up" algorithm for positions in which one side has a clear material advantage.

For further discussion of the evaluation routines the reader is directed to a chapter in reference 1 by David Slate and Larry Atkin in which they describe their program in some detail.

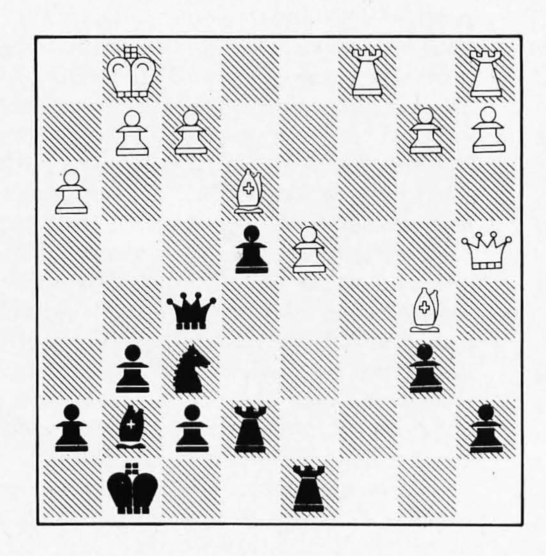
The CHESS 4.6 program plays extremely good chess. It is capable of beating 99.5 percent of all USCF rated players in the United States under tournament conditions. Perhaps even more remarkable is its play in blitz games. With restrictions of a five minute time limit for 60 moves, the program has already beaten many master players including David Levy, Hans Berliner and Lawrence Day. If any program has a chance to beat David Levy before next August, it will be CHESS 4.6. The authors will be working hard to improve the program between now and next summer.■

Game 1: White: DUCHESS. Black: KAISSA. For the record, here is the full listing of the victory of DUCHESS over KAISSA. In the first round of play, KAISSA was unexpectedly defeated by DUCHESS in an upset which will long be remembered. Post game analysis fingered a bug in KAISSA introduced by a last minute "improvement" of the program.

	White: DUCHESS	Black: KAISSA
1.	P-K4	P-Q4
2.	PxP	N-KB3
3.	P-Q4	NxP
4.	N-KB3	P-KN3
5.	B-K2	B-N2
6.	P-QB4	N-N3
7.	N-B3	O-O
8.	B-K3	B-N5
9.	P-B5	N-Q4
10.	O-O	P-K3
11.	Q-N3	P-N3
12.	NxN	PxN
13.	B-KN5	Q-Q2
14.	P-KR3	B-B4
15.	Q-B3	R-K1
16.	R-K1	B-K5
17.	N-Q2	Q-B4
18.	B-K3	Q-K3
19.	NxB	PxN
20.	PxP	BPxP
21.	R(K1)-QB1	. . .

Better is R(R1)-QB1. White has a positional advantage due to the control of the open file and the weak placement of Black's knight.

21.		N-Q2
22.	B-N4	Q-Q4
23.	Q-B6	N-B3
24.	B-K2	R(R1)-Q1
25.	Q-R4	R-K2
26.	B-N5	Q-KB4



Position after 26. . . Q-KB4.

This is the move which was apparently caused by a bug in the KAISSA program.

27.	R-B2	N-Q4
28.	R(1)-QB1	B-B3
29.	Q-N3	P-QR4
30.	P-KN4	Q-K3

Black's queen is terribly restricted.

31.	R-B6	P-R5

KAISSA sacrifices the rook pawn in order to draw DUCHESS' queen away from the long diagonal.

32.	QxP	R-Q3

The KAISSA program rejected Q-R8 as an important threat, and had consequently not fully analyzed the continuation which follows.

33.	RxR	QxR
34.	Q-R8ch !	R-K1

If 34. . . . K-N2, then 35. Q-B8ch KxQ, 36. B-R6ch B-N2, 37. R-B8, and mate follows.

35.	QxRch	K-N2
36.	P-N5	B-Q1
37.	B-QB4	Q-K2
38.	QxQ	NxQ
39.	B-B4	N-B4
40.	B-Q5	K-B1
41.	R-B8	K-K2
42.	R-B4	N-N2
43.	BxP	N-K3
44.	B-K3	N-B2
45.	P-Q5	N-N4
46.	B-B3	K-Q2
47.	P-QR4	N-Q3
48.	R-B6	N-B4
49.	BxP	Resigns.

weaker or untried programs. The previous world champion, KAISSA, from the Institute for System Studies in Moscow, was paired with ninth ranked DUCHESS from Duke University in Durham NC. It was expected that KAISSA would have an easy win.

Both KAISSA and DUCHESS utilize an "opening book" computer chess strategy. KAISSA's book contains 10,000 possible opening positions, whereas DUCHESS' book contains only 3,000. The use of an opening book allows the programs to play rapidly for the first few moves of each game while maintaining a line of play previously determined to be the best by human chess masters. Only two of the programs entered in the tournament played without opening books.

After 25 moves, the DUCHESS program, playing white, was judged by David Levy to have only a marginal positional advantage over black. To this point, KAISSA had used only 14 minutes of its available time while DUCHESS had used 59 minutes.

Under the rules of the tournament, each side must complete 40 moves in the first two hours, and at least ten moves in each succeeding half hour. Several programs, including KAISSA, made use of their opponents' time by preparing replies to the most probable move expected. Very often, the expected move would be played, and the program could respond instantly.

On move 26, KAISSA unexpectedly moved its queen from Q4 to B4. Although this move appeared to be of little significance, four moves later it became apparent that black was in trouble. KAISSA's black queen was dangerously restricted and DUCHESS was threatening checkmate. A rook sacrifice was necessary to prevent the immediate loss, but a win for black was almost impossible from that point onward. After move 48, DUCHESS was declared the winner, and the previous world champion

Note: *At the last minute, we discovered that BYTE's "automatic" chessboard drawing algorithm had used inverted logic, so please note that the chessboard diagrams in this article are all drawn with Black's home squares at the bottom (Sometimes we think we could use a little artificial intelligence)...*CM

Circle 106 on inquiry card.

had been upset in the first round by a previously unknown program.

It was learned the following day that the disastrous move had been the result of a bug in the program introduced when the programmers made last minute changes the evening before the tournament. The complete score of this game is printed in game 1, along with commentary.

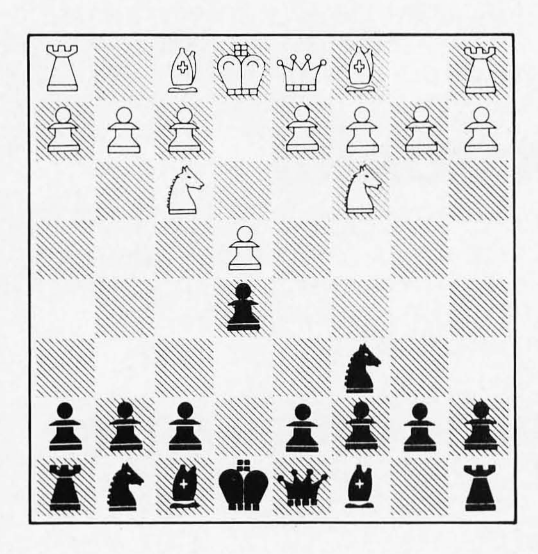


Figure 1: An interesting foible of the "opening book" strategy is revealed when a nonstandard opening occurs. In the game of DARK HORSE versus CHAOS, CHAOS was unable to recognize the transposed standard opening taken by DARK HORSE, and as a result it was thrown immediately into its middle game mode of operation. Here is the situation in DARK HORSE versus CHAOS after move 3, P-K4.

The tournament favorite, CHESS 4.6, met Don Beal's BCP in the first round of play. Due to a system failure, the CDC Cyber 176 used by CHESS 4.6 was not available at the scheduled start of play. Tournament rules allow each team up to 30 minutes of down time during which the chess clock may be stopped. When this period has expired, the clock must run and the time used is deducted from the two hours available for the first 40 moves.

CHESS 4.6 had almost an hour on their clock when service was restored. However, they wasted no time in defeating the English program in a rapid 27 move game which was the first game to end in the first round, despite the delays.

At the end of round one, CHESS 4.6, DUCHESS, CHAOS, MASTER, DARK HORSE, and OSTRICH had one point, BELLE, BLACK KNIGHT, ELSA, and BLITZ V had one half point, and the others had no points. For the second round, the programs all played against opponents with the same number of points from the first round.

KAISSA showed the strength it had not displayed in the first round, defeating TELL,

Results of the Second World Computer Chess Championships

n	Program	Round 1	Round 2	Round 3	Round 4	Total	Rank
1.	CHESS 4.6	1 (W,13)	1 (B,6)	1 (W,3)	1 (B,5)	4	1
2.	KAISSA	0 (B,3)	1 (W,16)	1 (B,4)	1 (B,7)	3	2
3.	DUCHESS	1 (W,2)	1 (B,11)	0 (B,1)	1 (B,6)	3	2
4.	CHAOS	1 (W,15)	½ (B,10)	0 (W,2)	1 (B,12)	2½	4
5.	BELLE	½ (W,7)	1 (B,12)	1 (W,10)	0 (W,1)	2½	4
6.	MASTER	1 (W,14)	0 (W,1)	1 (B,9)	0 (W,3)	2	6
7.	BLACK KNIGHT	½ (B,5)	½ (W,9)	1 (B,11)	0 (W,2)	2	6
8.	WITA	0 (B,11)	1 (B,13)	½ (W,15)	½ (W,10)	2	6
9.	ELSA	½ (W,12)	½ (B,7)	0 (W,6)	1 (B,15)	2	6
10.	DARK HORSE	1 (B,16)	½ (W,4)	0 (B,5)	½ (B,8)	2	6
11.	OSTRICH	1 (W,8)	0 (W,3)	0 (W,7)	½ (B,13)	1½	11
12.	BLITZ V	½ (B,9)	0 (W,5)	1 (B,14)	0 (W,4)	1½	11
13.	BCP	0 (B,1)	0 (W,8)	1 (B,16)	½ (W,11)	1½	11
14.	CHUTE 1.2	0 (W,6)	½ (B,15)	0 (W,12)	1 (B,16)	1½	11
15.	BS'66'76	0 (B,4)	½ (W,14)	½ (B,8)	0 (W,9)	1	15
16.	TELL	0 (W,10)	0 (B,2)	0 (W,13)	0 (W,14)	0	16

Table 1: The Second World Computer Chess Championships' results at a glance. In this table, each program's results in the four rounds of the tournament are summarized. A point (1) is awarded for each win, a half point (1/2) for each draw, and zero for each loss. In the notation of each round, the score color and opponent are given in the notation s (c,n) where s is the score for the round (1, 1/2 or 0), c is the color which the program played (B or W for black or white) and n is the number of the opponent in this list of programs.

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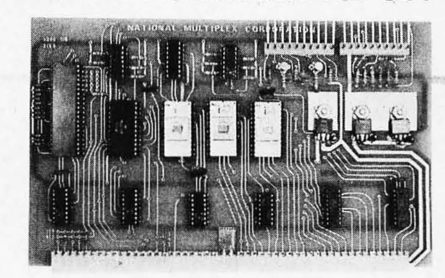
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from Switzerland, in a remarkable 16 moves, the shortest game of the tournament. TELL, written by Johann Joss, was European champion in 1975, and placed third in 1976.

In an interesting game, DARK HORSE, playing without the aid of an opening book, used a nonstandard opening against CHAOS, a program with an opening book of 7,500 positions. Since none of the book openings had prepared CHAOS for the very unusual N-QB3 move, it had to revert to its middle game analysis rather than responding instantly with a table lookup result. After three moves:

1. N-QB3 P-K4
2. N-B3 N-QB3
3. P-K4,

the position was transposed to a standard Four Knight's game usually obtained by:

1. P-K4 P-K4
2. N-KB3 N-QB3
3. N-B3.

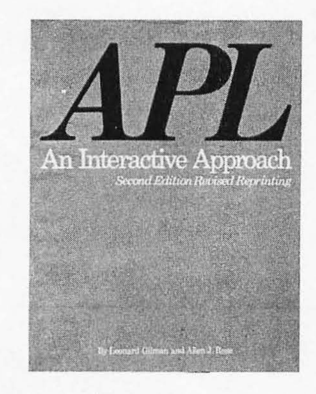
CHAOS, having discarded its opening table, was now unable to recognize that this was a standard position, and wasted precious time analyzing the position to determine the correct response (see figure 1).

At the end of the first two rounds of

Technical Comparisons								Author Information		
Rank	Program	Computer	Language	Program Size	Word Length	Opening Book	Average Number of Positions Examined per Move	Author(s)	Affiliation	Location of Computer
1	CHESS 4.6	CDC Cyber 176	Assembly	7.5 K + external core	60	5,600 positions	400,000	David Slate Larry Atkin	Northwestern University Evanston IL	Arden Hills MN
2	KAISSA	IBM 370/168	Assembly	250 K	32	10,000 positions	90,000	Dr M V Donskoy Dr V Arlazarov	Institute for System Studies Moscow USSR	Canada Systems Group Toronto, Ontario CANADA
2	DUCHESS	IBM 370/165	PL/I and Assembly	300 K	32	3,000 positions	1,200	Tom Truscott Bruce Wright Eric Jensen	Duke University Durham NC	Triangle Universities C C Triangle Park NC
4	BELLE	PDP-11 with chess hardware	"C"	8 K	16	10,000 positions	30,000	Ken Thompson Joe Condon	Bell Telephone Labs Murray Hill NJ	Bell Telephone Labs Murray Hill NJ
4	CHAOS	AMDAHL 470 V/6	FORTRAN	3 megabytes	32	7,500 positions	30,000	Mike Alexander T McBride Fred Swartz Bill Toikka Vic Berman Joe Winograd	University of Michigan Ann Arbor MI	Amdahl Corporation Sunnyvale CA
6	BLACK KNIGHT	UNIVAC 1110	FORTRAN	30 K	36	70,000 positions	7,500	Ken Sogge Fred Prouse Gary Maltzen Lonny Lebahn Elliot Adams	Sperry Univac St Paul MN	Sperry Univac Roseville St Paul MN
6	DARK HORSE	CDC 6600	FORTRAN	24 K	60	NO BOOK	12,000	Ulf Rathsman	Telefon AB LM Ericsson Stockholm SWEDEN	Multiple Access Computer Group Toronto, Ontario CANADA
6	ELSA	Telefunken TR440	Assembly	100 K	48	500 positions	---	Ludwig Zagler	Technischen Universitat Munchen WEST GERMANY	Technischen Universitat Munchen Munich WEST GERMANY
6	MASTER	IBM 370/168	PL/I	170 K	32	450 variations	100,000	J A Birmingham Peter Kent	Rutherford Lab and AERE Harwell, Oxfordshire UK	AERE Harwell UK
6	WITA	AMDAHL 470 V/6	ALGOL W	350 K	32	9,000 positions	250	Tony Marsland	University of Alberta Edmonton, Alberta CANADA	University of Alberta Edmonton, Alberta CANADA
11	BCP	CDC 6400	FORTRAN and Assembly	24 K	60	1,000 positions	1,000 per second	Don Beal	Queen Mary College London ENGLAND	McMaster University Hamilton, Ontario CANADA
11	BLITZ V	XEROX SIGMA 9	FORTRAN	24 K	32	5,000 positions	500	Robert Hyatt	University of Southern Mississippi Hattiesburg MS	University of Southern Mississippi Hattiesburg MS
11	CHUTE 1.2	AMDAHL 470 V/6	BPL (Extended XPL)	250 K	32	45 variations	900	Mike Valenti Zvonko Vranesic	University of Toronto Toronto, Ontario CANADA	Industrial Life Technical Services (IST) Montreal, Quebec CANADA
11	OSTRICH	Data General Supernova	Assembly	20 K	16	NO BOOK	10,000	Monroe Newborn George Arnold	McGill University Montreal, Quebec CANADA	At tournament site.
15	BS'66'76	IBM 370/168	FORTRAN	200 K	32	1,000 positions	150	Barend Swets	Private entry Tilborg NETHERLANDS	Datacrown Limited Toronto, Ontario CANADA
16	TELL	DEC KI10	ALGOL 60	15 K	36			Johann Joss	Eidgenossische Technische Hochschule Zurich SWITZERLAND	Dataline Systems Toronto, Ontario CANADA

Table 2: Technical characteristics of contestants. This table lists the major characteristics and source of each program entered into the Second World Computer Chess Championships. A total of 33 people were actively involved in the design and programming of the 16 programs entered in the contest; while no personally owned microcomputers were entered in the 1977 championships, we expect some future editions of the contest to include contestants from the world of personal computers.

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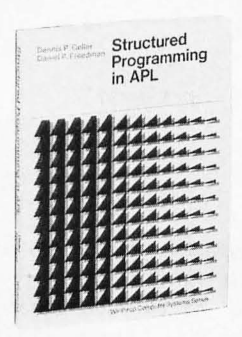
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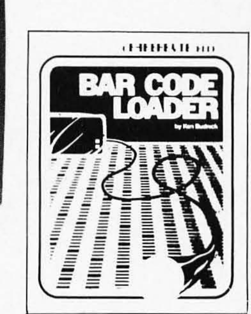


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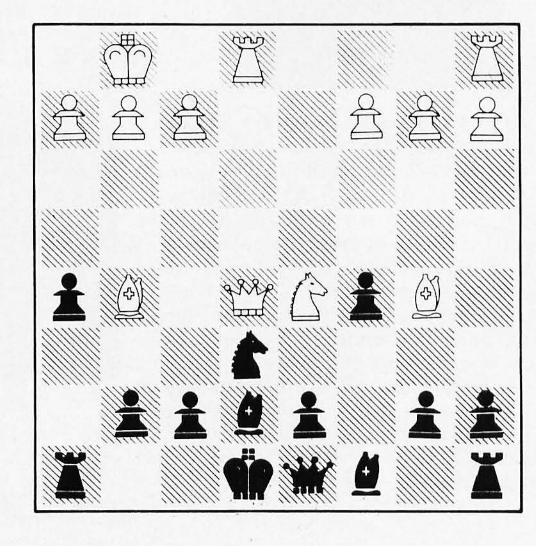
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White: KAISSA		Black: TELL
1.	P-K4	P-K4
2.	N-KB3	N-QB3
3.	B-N5	N-B3

The Berlin defense. As Fred Reinfeld pointed out, "The drawback of this once popular defense is that it leads to a weak pawn position for Black."

4.	O-O	NxP
5.	P-Q4	NxP
6.	NxN	PxN
7.	QxP	N-B4
8.	R-K1ch	N-K3
9.	N-QB3	P-QB4
10.	Q-K5	P-KR4?
11.	N-Q5	B-K2
12.	B-N5?	...



Position after 12. B-N5.

Game 2: The shortest game of the tournament was KAISSA's defeat of TELL in the second round.

12.	...	Q-R4
13.	BxB	P-QN3?
14.	QxNP	R-R3
15.	Q-N8ch	N-B1
16.	QxN mate	

play, only two programs, CHESS 4.6 and DUCHESS, had two wins to their credit. These two programs played each other in the third round. After a hard fought 50 move game, CHESS 4.6 extended its winning streak to three games.

Throughout the tournament, the moves of the OSTRICH program were punctuated by the familiar clatter of Monroe Newborn's ASR 33 Teletype, audible to the entire audience. On the sixteenth move of his game against BLACK KNIGHT, the Teletype began to clatter madly. It was obviously in an open loop. The cover was removed, and an urgent call was made for any ASR 33 experts in the audience. Unable to continue play, OSTRICH was forced to resign from the game. Later it was learned that, although the Teletype was making the noise, the fault lay with the serial IO interface of the minicomputer, and not with the terminal.

Problems were not confined to the on site minicomputer. In the final round of play, CHESS 4.6 was matched with BELLE, running on a PDP-11 located at the Bell Telephone Laboratories in Murray Hill NJ. The game was interrupted for several minutes because BELLE was experiencing communications difficulties.

An interesting aspect of the BELLE system was the use, for the first time, of a microprogrammed hardware move generator added to the PDP-11. This feature allowed a much faster generation of positions for analysis and is thought by many to be the route to better chess playing computers. In this case, it was not enough. After 52 moves, CHESS 4.6 mated BELLE to win the game, and the tournament.

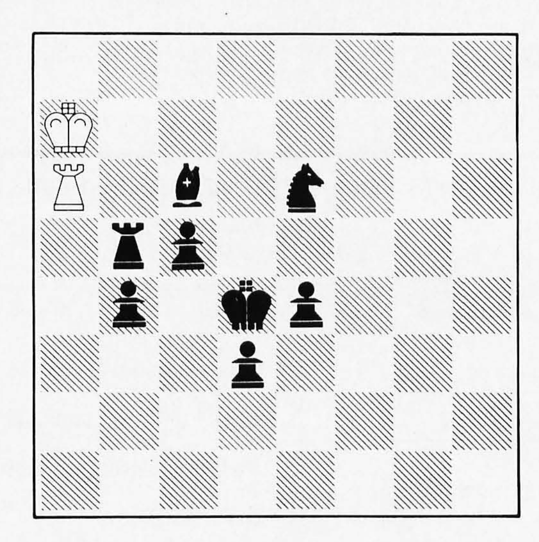
The final results, shown in table 2, show that CHESS 4.6 was the undisputed champion with four wins, KAISSA and DUCHESS tied for second with three wins each, and CHAOS and BELLE tied for third with two wins and a draw each.

Prizes of another sort went to the following programmers and their programs:

1. One programmer inserted (just for fun) a message into his program to print "POSSIBLE MATE IN x MOVES" each time a mate threat was discovered in the analysis. When the position became dangerous during round 1, the number of possible mate threats became enormous. The programmer was unable to interrupt the program as it listed page after page of possible mate combinations in 2, 3, 4, ... 16 moves. As a result, the opponent's move could not be entered and the game was lost due to a time forfeit. None of the mate threats were irrefutable. By round 2, the message had been removed.
2. A bug in another program was not a new one. It had been in the program for nearly ten years. Unable to locate the exact cause of a fatal run time error which occurred sporadically during the program execution, the programmer devised a subtle solution to prevent the program from abending during a game by trapping the error code before the operating system could react to it and initiating an error recovery routine which would restart the program and skip the error prone analysis. A message was directed to the line printer to inform the programmer that the recovery routine had been called. This procedure had allowed the program to compete successfully in several tournaments without a single fatal abend. During

Game 3: The final game of the tournament was BELLE versus CHESS 4.6, listed here.

	White: BELLE	Black: CHESS 4.6
1.	P-K4	N-QB3
2.	N-KB3	P-K3
3.	P-Q4	P-Q4
4.	N-B3	B-N5
5.	P-K5	N/1-K2
6.	P-QR3	BxNch
7.	PxB	N-R4
8.	B-N5ch	B-Q2
9.	B-Q3	R-QB1
10.	N-N5	P-KR3
11.	N-B3	P-QB4
12.	PxP	RxP
13.	B-K3?	RxP
14.	BxQRP	N-B5
15.	O-O	RxRP
16.	RxR	NxR
17.	B-QB5	Q-R4
18.	B-Q6	N-B5
19.	Q-R1	N-B3
20.	QxQ	N/3xQ
21.	R-R1	B-B1
22.	P-B3	N-B3
23.	R-R4	NxB
24.	PxN	K-Q2
25.	R-KN4	P-KN4
26.	B-B2	KxP
27.	R-QR4	P-N4
28.	R-R1	P-QN5
29.	PxP	NxP
30.	B-N1	B-Q2
31.	K-R1?	P-B4
32.	N-Q4	R-QB1
33.	N-K2?	B-N4
34.	N-N1	R-B8
35.	R-R5	RxB
36.	P-B3?	B-B8
37.	P-R4?	R-N7
38.	PxP	BxPch
39.	K-R2	PxP
40.	R-R4?	BxPch
41.	K-N3	B-R4
42.	K-R3?	P-B5
43.	R-R8	B-N3
44.	K-N4	R-N7ch
45.	K-R3	RxN
46.	K-R2	R-N5
47.	R-Q8ch?	K-K4
48.	R-KN8?	B-K5
49.	R-N7?	B-B6
50.	R-KR7	N-Q6
51.	R-R3?	. . .



Position after 51. R-R3?

51.	. . .	R-N7ch
52.	K-R1	N-B7mate

round 1, the error recovery routine was called three times. In round 2, it was called ten times; in the third round, 20 times. But in round 4, the position of the game somehow triggered a tight loop around the patched code. The run time error was triggered 800,000 times. The error recovery routine was called 800,000 times, and 800,000 lines of printed output awaited the programmer at the data center the next day. The program did not abend, but it also did not win. It probably spent most of its time in the error recovery routines.

The standard of play evidenced by the programs competing in this tournament shows considerable improvement over that demonstrated three years ago in Stockholm at the First World Computer Chess Championships. Still, no program available at this time is capable of defeating a master ranked player in regular play. Room for improvement still lies in the need for the incorporation of long range plans into the computer chess algorithms. This is an aspect of chess play which is vital to good human strategy and yet completely lacking from all conventional computer chess programs.

Also needed are some fundamental improvements in the end game play of the programs. Most of the current algorithms suffer the consequences of the "horizon effect," a term coined to describe the blunders made when a program fails to see threats or opportunities one or more levels below the maximum number of plies it has searched. This is a particular problem in end game strategy, where short term heuristics are not necessarily relevant to the winning combination.

Current advances in artificial intelligence, pattern recognition and multiprocessors are likely to enable significant improvements in the chess ability of future computer systems over the next few years. It is now quite conceivable that master level play will be achieved within this decade, and yet it is still entirely possible (if not probable) that grand master play will not be achieved in this century.■

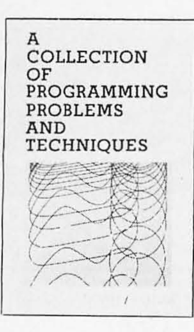
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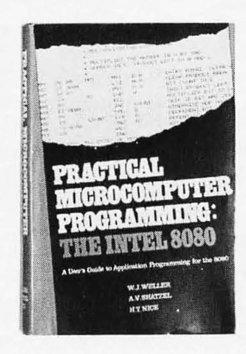
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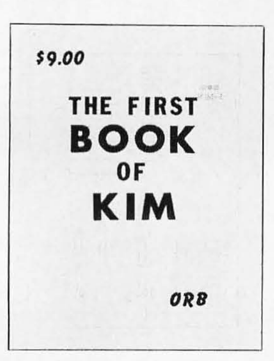
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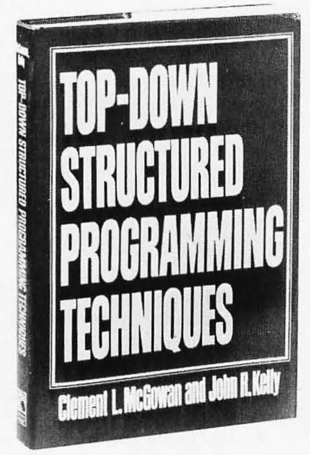




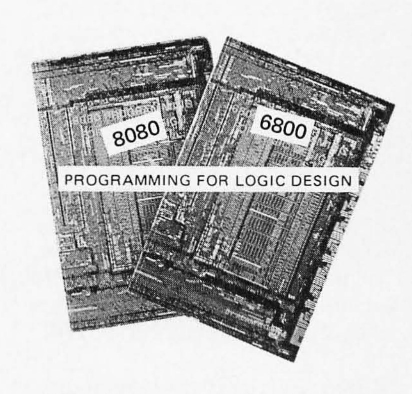
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NCC Personal Computing Festival

A Personal Computing Festival will share the public spotlight in conjunction with the 1978 National Computer Conference to be held June 5-8 in Anaheim CA. A call for papers has been issued for the Festival program to be held June 6-8 at the Disneyland Hotel adjacent to the Anaheim Convention Center. Included as part of the 3 day program will be presentations of invited papers, contributed papers, and tutorials, as well as panel discussions relevant to personal computing. Letters of intent to participate as either an author, panelist or session chairperson must be submitted by February 1 1978. Authors who have received notification of acceptance must submit final papers by March 15 1978 in a specified camera ready format.

Chairperson of the Festival program is Jim C Warren Jr, editor, *Dr Dobb's Journal of Calisthenics and Orthodontia,* Woodside CA. According to Warren, approximately 30 sessions are planned with emphasis on the following areas, although papers and session proposals on other topics are encouraged:

- Tutorials for computer novices.
- Speech synthesis and speech recognition.
- Computer driven and computer assisted music systems.
- Computer graphics and video art.
- Personal computers for the physically disabled.
- Personal computers for education.
- Business systems using "home" computers.
- Hardware and software design and implementation.
- Standards for hardware, interfaces and software.

Papers presented during the Festival program will be published in a softbound book, *Festival Digest 78,* which will be available during the NCC.

Potential authors should immediately send a "letter of intent" including an abstract of their proposed talk to: Jim C Warren Jr, Star Route POB 111, Redwood City CA 94062; (415) 851-7664. Festival author kits, which will be mailed to authors, contain instructions and the necessary materials for preparing the camera ready copy.

Session chairpersons must submit two copies of a 250 word abstract describing the scope of the proposed sessions and tentative title of presentations by February 1 1978. In the case of panel sessions, the prospective organizer should list proposed panelists, their titles and affiliations, and a brief biography of each speaker. Prospective session chairmen will be notified as to the disposition of suggested sessions by February 10 1978.

In addition to the Festival program, there will be an exhibit of personal computing products and services and an exhibition of individually designed home and hobby computers and applications.

Information on NCC 78 may be obtained from AFIPS, 210 Summit Av, Montvale NJ 07645 or by calling (201) 391-9810.■

When Is ASCII Not ASCII?

One reader recently wrote in complaining that a product advertised as an ASCII keyboard was in his opinion not an ASCII keyboard at all. ASCII is the American Standard Code for Information Interchange, a 7 bit definition of data and command codes maintained by ANSI, the American National Standards Institute. The crux of this reader's comment about the product in question is that:

- First, the keyboard in question only defined an ASCII subset.
- Second, the control sequences generated by this keyboard were not what he wanted.

To the first point, one might comment that rare is the keyboard which can generate all 128 possible codes of an ASCII set; it is sometimes hard enough finding one which gives both upper and lower case. But just because the full ASCII set is not generated does not mean that we don't have an ASCII keyboard. If the keyboard generated EBCDIC (Extended Binary Coded Decimal Information Code, IBM's nonASCII code) or other codes, then it could validly be said not to be an ASCII keyboard; but this reader's keyboard did indeed put out ASCII codes for ASCII graphics. To the second point, one might comment that the ASCII definition says nothing about how the codes are generated in a particular piece of hardware. In many instances, the CTRL key does indeed act as a shift key of sorts, but this is not the only possible way to generate control character values in hardware given human inputs.■

An Interesting Point About the State of Computer Technology

In a recent conversation, Stephen M Hicks of FORTH Inc made an interesting point about personal computers and the present state of public awareness of technology: the personal computer viewed as a toy is to present day technology what the "erector set" was to mechanism and structural technology in an earlier era. When mechanical construction toys first caught on, the public was aware of numerous examples of existing structure in transportation and general industry that could be modeled and emulated through the learning device of the construction toy. Viewing the personal computer as an educational toy, the present day consumer has a means of learning about and understanding what goes on in computer systems (which are seen throughout industry and commerce today) via working examples of programs and applications. This general awareness of computer systems and their extensive effects is perhaps part of the widening public fascination with computers. . .CH ▪

ACM's New Special Interest Group on Personal Computing

The Association for Computing Machinery has chartered a new Special Interest Group on Personal Computing called SIGPC. SIGPC will be operated exclusively for educational and scientific purposes in the design and applications of computer systems for home, clerical, small business, management and recreational uses. It also includes the technology of such systems in software and hardware, and emphasizes techniques appropriate to the integration of such tools as graphics, speech, data management and music systems. Dr Portia Isaacson, who chaired the 1977 National Computer Conference, has been appointed chairperson of SIGPC. To join SIGPC, write to the Association for Computing Machinery, POB 12105, Church Street Sta, New York NY 10249. ▪

Structured Programming with Warnier-Orr Diagrams

Part 2: Coding the Program

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Langston Kitch and Associates
715 E 8th St
Topeka KS 66607

In part 1 we carefully constructed a design structure. In order to make the most of that structure a few words about programming style are in order. While it is true to a certain extent that any method of coding the structure will produce a logically correct program, matters of syntactical errors resulting from shoddy coding techniques as well as problems with *maintainability* seem to indicate that a great deal of care should be exercised in the construction of the actual program code.

For this particular example, I'll use a fairly standard version of BASIC that

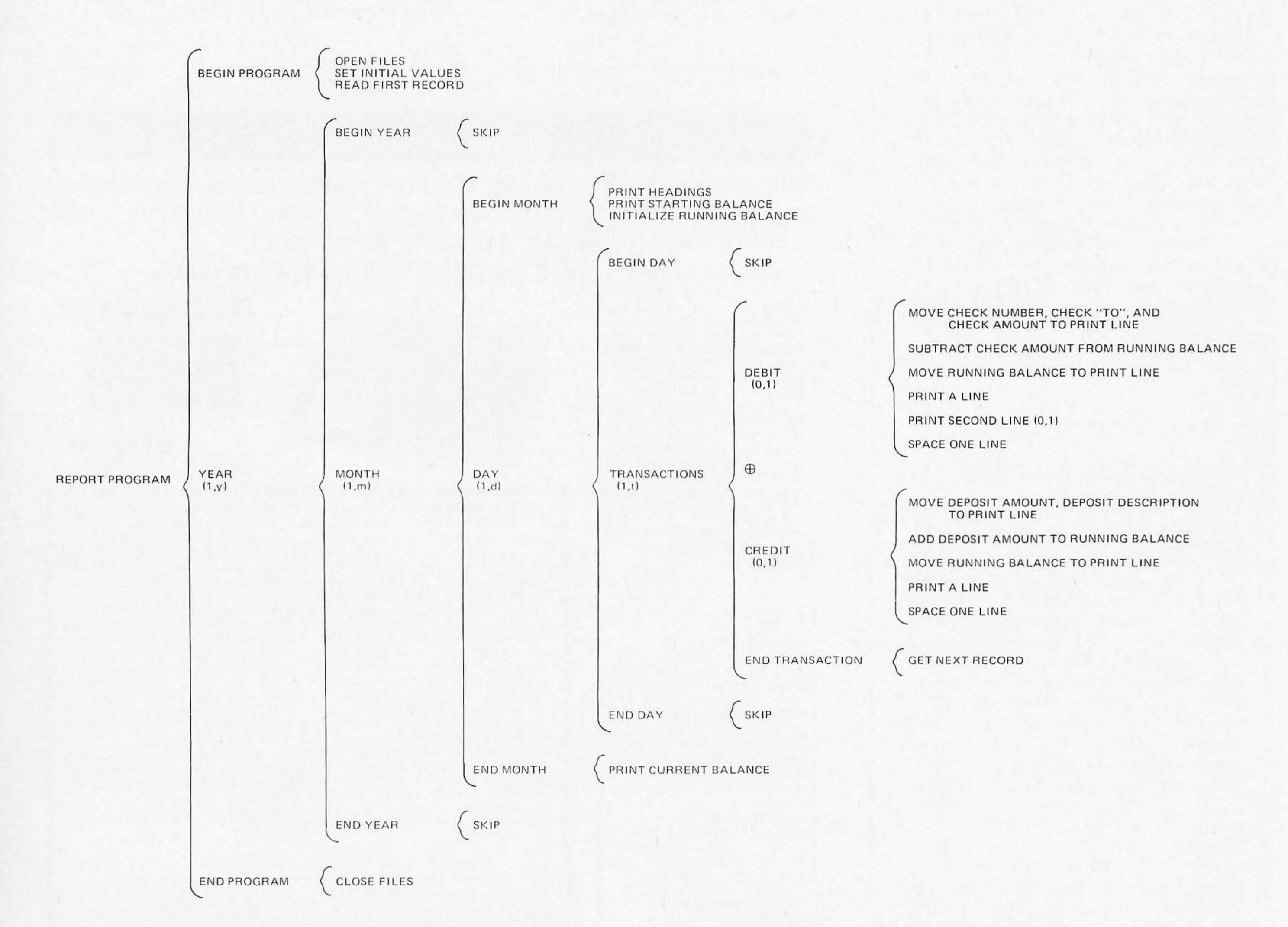


Figure 1: Final Warnier-Orr diagram description of the checkbook balance report program (reproduced from part 1).

runs on a J100 Jacquard Systems computer. The concepts and construction rules are just as applicable to Tiny BASIC, assembly language, and especially APL. Obeying the following five coding conventions will help you write a program that will execute on the first time.

Coding Convention 1: Names Should Be Indicative of Function

For versions of BASIC that only allow one letter names, this is often a little hard, but for most other languages with multiple character symbols, it is a must. For instance, a field that contains an amount should be labeled AMOUNT, an address field should probably be called ADRESS, and so forth. Cutesy names: SNEEZY, DOPEY, GRUMPY, HELL (a perennial favorite label for adolescent COBOL programmers) are to be strictly avoided.

Coding Convention 2: Comments Should Be Used Freely

Comment lines in programs written in obscure languages, APL for instance, should probably outnumber actual lines of code. Comment lines are especially useful for explaining unclear methods of calculation, complex decisions, etc.

Coding Convention 3: Every Bracket of a Warnier-Orr Diagram Should Represent a New Subroutine

Languages that do not permit subroutines or languages that limit the levels of nesting of subroutines are very tricky to use and should be avoided if at all possible. Save your spare change for three or four weeks and go buy a better version of BASIC; there are plenty of good ones on the market. In BASIC, each subroutine should be clearly labeled with REMark statements.

Coding Convention 4: Subroutines Should Be as Short as Possible

If a subroutine contains too many statements it is difficult to understand and maintain. It also means you are probably doing something in this subroutine that should be put in another subsequent subroutine. In most high level languages a practical limit of 10 to 20 statements is appropriate.

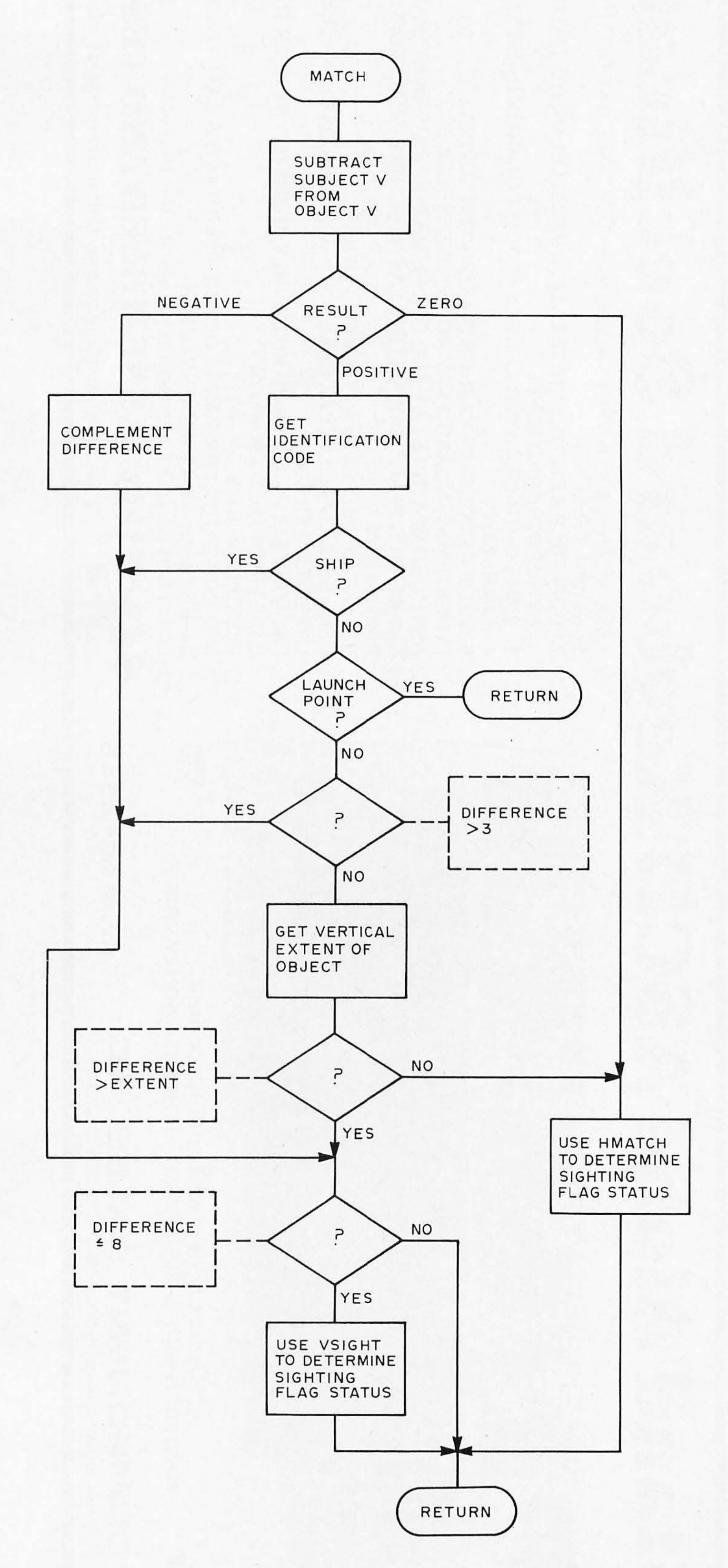


Figure 2: This a a flowchart chosen at random for comparison to a Warnier-Orr representation.

This rule is standard structured programming practice.

Coding Convention 5: GO TOs Should Be Avoided

In higher level languages, GO TOs can often and should be eliminated entirely. However, in versions of BASIC that do not have a DO verb and in assembler, GO TOs are often necessary. Utmost care is urged whenever a GO TO is used; it should only be used as a last resort. In assembly language, use of arbitrary jumps or branches should be avoided.

When coding the program, the order of the subroutines is not crucial. The only piece of code that must be fixed in any certain location is the highest level bracket which must be the first executable line, or lines, of code. One possible way of coding the first section is to omit the first bracket and consider the code as the main program. For BASIC, subroutine calls are left unnumbered until the subroutine is actually written. In this case, we use nnn to indicate an unknown number.

```
100 REM CHECKBOOK BALANCE REPORT PROGRAM

110 REM     BEGIN PROGRAM
120         GOSUB nnn

130 REM     YEAR (1,Y)
140         LET ENDYR = FALSE
150         GOSUB nnn
160         IF ENDYR = FALSE THEN GOTO 150

170 REM     END PROGRAM
180         GOSUB nnn
190         END
```

Another way to program this section would be to have the above piece of code as a subroutine to an even higher level procedure as follows.

```
80 REM CHECKBOOK BALANCE REPORT PROGRAM
90 GOSUB 110
95 END
   .
   . 100 through 180 as above
   .
200 RETURN
```

Either way of coding is acceptable. Note that the GO TO in statement 160 is used to create the structure of a DO UNTIL, a feature that is not available with this particular BASIC.

The center path of the Warnier-Orr diagram is the easiest to begin to code at this point. So the code for the YEAR, the MONTH, and the DAY routines is shown next; for the subroutine YEAR:

```
250 REM YEARLY PROCEDURE

260 REM     BEGIN YEAR
270         GOSUB nnn

280 REM     MONTHS (1,M)
```

```
290        LET ENDMO = FALSE
300        GOSUB nnn
310        IF ENDMO = FALSE THEN GOTO 300

320 REM    END YEAR
330        GOSUB nnn
340        RETURN
```

For the subroutine MONTH:

```
350 REM MONTHLY PROCEDURE

360 REM    BEGIN MONTH
370        GOSUB nnn

380 REM    DAYS (1, D)

380 REM    DAYS (1,D)
390        LET ENDAY = FALSE
400        GOSUB nnn
410        IF ENDAY = FALSE THEN GOTO 400

420 REM    END MONTH
430        GOSUB nnn
440        RETURN
```

For the subroutine DAY:

```
450 REM    DAILY PROCEDURE

460 REM    BEGIN DAY
470        GOSUB nnn

480 REM    TRANSACTIONS (1,T)
490        LET ENDTRN = FALSE
500        GOSUB nnn
510        IF ENDTRN = FALSE THEN GOTO 500

520 REM    END DAY
530        GOSUB nnn
540        RETURN
```

The TRANSACTIONS process breaks down as follows:

```
550 REM    TRANSACTIONS ROUTINE

560 REM    CREDIT (0,1) OR DEBIT (0,1)
570 IF CDFLAG = CREDIT THEN GOSUB nnn ELSE GOSUB nnn

580 REM    END TRANSACTION
590        GOSUB nnn
600        RETURN
```

Subroutine DEBIT is coded a bit differently from the way it was designed for one simple reason. BASIC will let you output from the same fields that were read in as input; many languages do not. Therefore, the only code remaining in the subroutine is the subtraction of the amount from the running balance and the print commands.

```
610 REM DEBIT PROCEDURE
620     LET RUNBAL = RUNBAL - AMOUNT
650     PRINT ON PRINTR: DAY, CHKNUM, DESC1, DRAMT, CRAMT, RUNBAL
660     IF DESC2 # SPACES THEN PRINT ON PRINTER: DESC2
670     PRINT ON PRINTR: SPACES
680     RETURN
```

The symbol # is the not equal to operator. Note that this code makes no attempt to format the output line. Although the facility is available with this version of BASIC, it *differs* greatly from other line formatting BASICs around, and would serve only to confuse the immediate issue.

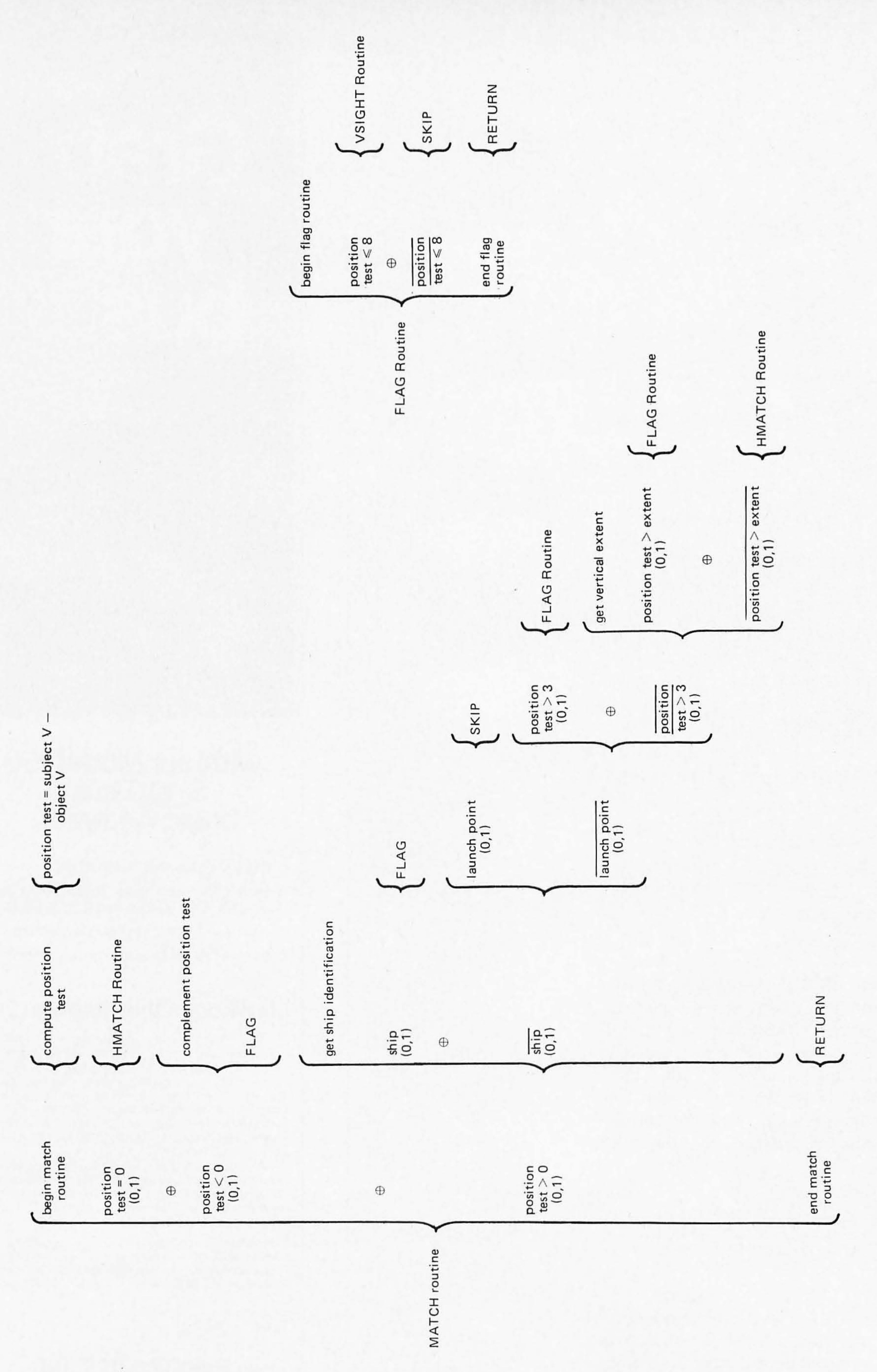


Figure 3: The original flowchart converted into Warnier-Orr diagram. This is a much simpler looking diagram and is easier to follow and explain to someone. Since it is broken down into sections it can be programmed as a series of subroutines that can be easily maintained and modified.

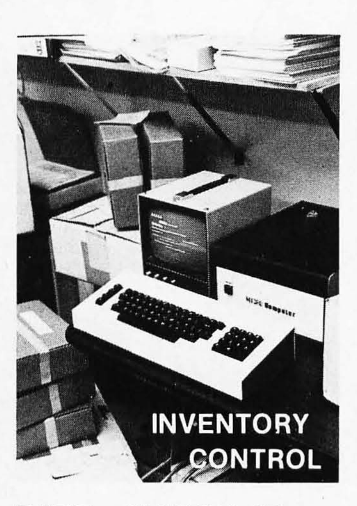
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The CREDIT process is very similar to the DEBIT process.

```
690 REM    CREDIT PROCEDURE
700        LET RUNBAL = RUNBAL + AMOUNT
730        PRINT ON PRINTR: DAY, DESC1, CRAMT, DRAMT, RUNBAL
740        PRINT ON PRINTR: SPACES
750        RETURN
```

The only remaining subroutines to be coded appear below:

```
760 REM    END TRANSACTION
763        LET OLDDAY = DAY
770         INPUT FROM CHECK1: DAY, CDFLAG, DESC1, DESC2,
           CHKNUM, & AMOUNT
775        ON ENDFILE GOSUB nnn
778        IF OLDDAY # DAY THEN LET ENDAT = TRUE
780        RETURN

790 REM    END OF CHECK FILE DEFAULT SUBROUTINE
800        LET ENDAY, ENDTR, ENDMO, ENDYR = TRUE
810        RETURN

820 REM    BEGIN MONTH PROCEDURE
830        PRINT ON PRINTR: HDR1$
840        LET RUNBAL = BALANC
850        PRINT ON PRINTR: RUNBAL
860        PRINT ON PRINTR: HDR2$
870        PRINT ON PRINTR: SPACES
880        RETURN

890 REM    END MONTH PROCEDURE
900        PRINT ON PRINTR: RUNBAL
920        RETURN
```

The program is finished with the BEGIN PROGRAM and the END PROGRAM subroutines, which are not developed here, and the replacing of the untagged GOSUBs coded before. The modules for which a GOSUB was generated should probably remain a part of the program even though they contain no code. They make maintenance much easier. The entire working program with formatting and other embellishments appears in listing 1.

Conclusion

The art of programming has become a process which can be taught to anyone who needs to use it, which is something that we have not been able to accomplish until very recently. Admittedly, the technique for developing programs presented here is sometimes tedious and not very creative, but it will get the job done. In the personal computer field a lot of enthusiasts probably enjoy programming on the fly and spending all night debugging. But for those who don't, including myself, and who aren't satisfied with just running someone else's canned programs, there is an alternative. As the pioneer in this methodology, Jean-Dominique Warnier, puts it: "If you don't have time to do it right, do you have time to do it over?" Realistically, one cannot say that this methodology is the ultimate in software process design or that it is completely right. It is not. Something is sure to come along in the future that is better. But, for now, it is certainly a large step in the right direction.

Listing 1: BASIC source listing for the checkbook balance report program. Each of the subroutines can be matched with one of the brackets in the diagram of figure 1. The individual modules that do not contain any code should be left as they are to facilitate easy maintenance in the future.

```
100 REM CHECKBOOK BALANCE REPORT PROGRAM
110
120 REM     BEGIN PROGRAM
130         GOSUB 1090
140
150 REM     YEAR (1,Y)
160         LET ENDYR = FALSE
170         GOSUB 280
180         IF ENDYR = FALSE THEN GOTO 170
190
200 REM     END PROGRAM
210         GOSUB 1290
220         END
230
240 REM ****************************************
250 REM YEARLY PROCEDURE
260
270 REM     BEGIN YEAR
280         GOSUB 1470
290
300 REM     MONTH (1,M)
310         LET ENDMO = FALSE
320         GOSUB 430
```

Once I finished reading about the ease with which Warnier-Orr diagrams could be used I decided to take a sample flowchart and convert it into the Warnier-Orr form to see how much of a difference there actually was. I happened to be working on an article by Geoffrey Gass (entitled "Starfleet") which contained a large number of flowcharts. Choosing one at random I converted it. Figure 2 is the original flowchart. Figure 3 is the converted diagram. I think the Warnier-Orr form is much easier to read and understand.

When designing with flowcharts it is sometimes difficult not to cross lines or have a great deal of redundancy in the program which makes it difficult to follow. All the arrows going across the paper are very distracting and hard to follow. The Warnier-Orr diagram does not have this disturbing problem. It is very easy to follow the program through the various subroutines.

The Warnier-Orr diagram lends itself to structured program writing. If you consider each of the separate brackets another subroutine it is very easy to write the program just as it stands from top to bottom. When we use conventional flowchart techniques we end up leaping about the program to perform statements that are at various parts of the same routine. In my opinion the Warnier-Orr diagram is a quantum leap in the direction of aid for structured program designers.

Ray Cote
Coop Editor

Listing 1, continued:

```
330         IF ENDMO = FALSE THEN GOTO 320
340
350 REM     END YEAR
360         GOSUB 1390
370         RETURN
380
390 REM ****************************************
400 REM MONTHLY PROCEDURE
410
420 REM     BEGIN MONTH
430         GOSUB 1210
440
450 REM     DAYS (1,D)
460         LET ENDAY = FALSE
470         GOSUB 580
480         IF ENDAY = FALSE THEN GOTO 470
490
500 REM     END MONTH
510         GOSUB 1340
520         RETURN
530
540 REM ****************************************
550 REM DAILY PROCEDURE
560
570 REM     BEGIN DAY
580         GOSUB 1500
590
600 REM     TRANSACTIONS (1,T)
610         LET ENDTR = FALSE
620         GOSUB 720
630         IF ENDTR = FALSE THEN GOTO 620
640
650 REM     END DAY
660         GOSUB 1430
665         RETURN
670
680 REM ****************************************
690 REM TRANSACTIONS PROCEDURE
700
710 REM     CREDIT (0, 1) OR DEBIT (0, 1)
720         IF CDFLAG = DEBIT THEN GOSUB 800 ELSE GOSUB 890
730
740 REM     END TRANSACTION
750         GOSUB 965
760         RETURN
770
775 REM ****************************************
780 REM DEBIT PROCEDURE
790
800         LET RUNBAL = RUNBAL - AMOUNT
810         PRINT :DAY;CHKNUM;DESC1;'     ';AMOUNT;RUNBAL
820         IF DESC2 # ' ' THEN PRINT :SPACES;DESC2
830         PRINT :SPACES
840         RETURN
850
860 REM ****************************************
870 REM CREDIT PROCEDURE
880
890         LET RUNBAL = RUNBAL + AMOUNT
900         PRINT :DAY'      ';DESC1;AMOUNT;'      ';RUNBAL
910         PRINT :SPACES
920         RETURN
930
940 REM ****************************************
950 REM END TRANSACTION
960
965         LET OLDDAY = DAY
970         INPUT FROM CHECKS:DAY,CHKNUM,CDFLAG,DESC1,DESC2,AMOUNT
980         ON ENDFILE CHECKS GOSUB 1030
985         IF OLDDAY # DAY THEN LET ENDAY = TRUE
990         RETURN
1000
1010 REM ***************************************
1020 REM END OF FILE
1025
1030        LET ENDAY, ENDMO, ENDTR, ENDYR = TRUE
1040        RETURN
1050
1060 REM ***************************************
1070 REM BEGIN PROGRAM PROCEDURE
1080
1090        OPEN 'CHECKS',SYMBOLIC,INPUT:CHECKS
1100        STRING SPACES, CDFLAG, DESC1, DESC2, MONTH
1110        DECIMAL AMOUNT, BALANC, RUNBAL
1120        LET TRUE = 1
1130        LET FALSE = 1
1140        LET SPACES = '
1150        INPUT FROM CHECKS: DAY, CHKNUM, CDFLAG, DESC1, DESC2,
            AMOUNT, BALANC, & MONTH, YEAR
1160        RETURN
1170
1180 REM ***************************************
1190 REM BEGIN MONTH
1200
1210        PRINT :'              CHECKBALANCE REPORT'
1220        PRINT :'        FOR THE MONTH OF ':MONTH;YEAR
1230        PRINT :SPACES,'BALANCE FORWARD OF ';BALANC
1235        LET RUNBAL = BALANC
1240        PRINT :'DAY CHECK# FOR            DEBIT CREDIT BALANCE'
1250        RETURN
1260
1265 REM ***************************************
1270 REM END PROGRAM
1280
1290        CLOSE CHECKS
1300        RETURN
1310
1315 REM ***************************************
1320 REM END MONTH
1330
1340        PRINT :'CURRENT BALANCE ',RUNBAL
1350        RETURN
1360
1365 REM ***************************************
1370 REM END YEAR
1380
1390        RETURN
1400
1405 REM ***************************************
1410 REM END DAY
1420
1430        RETURN
1440
1445 REM ***************************************
1450 REM BEGIN YEAR
1460
1470        RETURN
1480
1485 REM ***************************************
1490 REM BEGIN DAY
1495
1500        RETURN ■
```

Continued from page 36

erally seek to learn all they can concerning the field. They might look for news of the latest accomplishments, so that they may avoid pointless repetition of discoveries and innovations already made.

I too would like to make a robot move, and recognize patterns, and play with blocks. With the knowledge that I am not equipped for such an endeavor, I am highly pleased to learn of the accomplishments of others.

In another light, many people seem to be missing the true meaning of artificial intelligence. Richard Rosenbaum, in the April 1977 BYTE, declares that artificial intelligence is simply "the substitution of a computer (artificial mechanism) for what are ordinarily human tasks (generally assumed to require intelligence)." I must disagree.

The problem comes in defining intelligence.

In having the computer perform simple operations, such as the four operations of arithmetic, are we not substituting a computer for a human task? Is this artificial intelligence? It is rather simulated intelligence. The computer appears to be operating like a human mind. However, the computer employs a sequence of "mechanical" operations to arrive at a solution to the arithmetic problem. The human mind makes use of previously compiled knowledge, reorganizing it. The computer generates new data.

With consideration, one realizes that most human mental functions are based upon the manipulation of stored information. As data is received through the sensory systems, it is placed in the mind in the order perceived. As comparisons are made the information is copied into other areas of the brain. Associated images are stored together. Collections of data are called out again when the senses receive a piece of information common to the group. Mental structures grow and are enhanced constantly; so grows the mind from the moment of birth to the instant of death.

Obviously, present day experimenters' computers do not have the capacity to handle information on the same scale

as the human mind. However, all animal minds seem to function in essentially the same manner. As a matter of observation, emotional capacity and intelligence seem to have a direct relationship to the physical size of a particular species' brain. It may be possible to synthesize the mental functions of less intelligent animals; insects, rodents, primates. One might even consider synthesizing the infant human mind. While we may not actually create complete minds, it is possible to develop the basic foundations of self evolving intelligence.

Innovations in cybernetics are making it possible to give the computer necessary perceptual input. Vocal input and output devices and digital "eyes" are making it possible for the computer to hear, see, and stimulate its environment in order to obtain new information.

I would like very much to communicate with anyone interested in the study of artificial intelligence. Perhaps by coordination of efforts we can make more rapid progress.

Scott Jarol
3401 E Shaw Butte Dr
Phoenix AZ 85028

MORE MUSINGS ON AI'S WHYS

I have been reading with some interest the ongoing discussion in "Ask BYTE" of the relative merits of artificial intelligence and robots. I feel however that all sides have missed the central question which is: what effect can we reasonably expect the microcomputer or, for that matter, any new tool or technique to have on the quality of human life?

On one extreme is the possibility that the great increase in productivity for the average worker which will result from use of microcomputers will allow us to enjoy a significantly better standard of living than would be otherwise possible. At the other extreme is the probability that this same increase in productivity will enable us to support the ever increasing masses of humanity, which are already almost beyond imagining, without measurable benefit to ourselves.

The central question, stated in its simplest form, is an old one. Who do you feed first, your family or someone else's?

As for artificial intelligence, the raw materials (a monolithic central processor and monolithic mass memory) are already available and the incentives become stronger daily as human workers price themselves out of the market. My only hope is that the robots we develop will be offspring we can be proud of.

Mark Williamsen
607 Barton Av
Evanston IL 60202

GETTING UV BULBS

The article on the "Coffee Can Special" (January 1977 BYTE, page 91) by Lawrence Burbey Jr failed to mention the type of lamp to use.

We built a similar device months ago and after much difficulty we found the GE#G 4511 lamp was cheap, worked well and was relatively easy to obtain.

Stephen Pumple
The Computer Place
186 Queen St W
Toronto CANADA M5V 1Z1

D1 or D2?

Your response to Paul E Pennington in the September 1977 BYTE *[page 178]* contains an error. The Motorola MEK6800D1 does contain the MIKBUG monitor. The Motorola MEK6800D2 contains the JBUG monitor. I am sure of this since I possess both units.

J C Hausler
67 Fisher Rd
Rochester NY 14624

A NORTH GERMAN COMPUTER CLUB?

Call for interested individuals in (northern) Germany to form a hobbyist computer club. Please contact Ilja Burkoff, Parkallee 105, D-28 Bremen. Tel: (0421) 347179.

Since your magazine is being read internationally, could you coax your advertisers into leaking the names and addresses of foreign dealers and distributors in their ads?

Ilja Burkoff
Management Consultant
Parkellee 105
D-28 Bremen W GERMANY

TYPEBALLS

In the October 1977 BYTE (page 12) you seem to be answering a question that reader Rob Loring really wasn't asking. If I read his letter correctly, he was asking where he could buy a Selectric typeball with both human readable characters and also machine readable bar codes. Nowhere did he say he wanted to *design* one, he just wanted to *buy* one. IBM sells at least two such typeballs for the quite reasonable price of $24 each. Both have upper and lower case plus numerals and special characters. If neither of these will do the job, there are at least three others available, at $32 each, from the Datatype Corporation, 1050, N W 163rd Dr, Miami FL 33169, (305) 625-8451. There is certainly no need whatever to reinvent the wheel, or the typeball.

Jim Day
17042 Gunther St
Granada Hills CA 91344

The balls IBM and Datatype sell are optically encoded, yes, but not in the format of the bar codes used in our Paperbyte™ software representations. The availability of the IBM optically scannable fonts was brought home to

me when I ordered a couple of new balls for my Selectric from the IBM office products sales brochure. Aside from optical character recognition (OCR) compatible fonts, IBM offers a font with a unit bar code printed below each letter . . .CH.

MORE ABOUT -ILLION

The origin of billion, according to the *Concise Oxford Dictionary,* is "French, coined in the 16th century out of bi- & million to denote the second power of a million; meaning afterwards changed in France (so US) but not in England."

Great Britain and Germany know a "thousand million" as a "milliard." But why stop there? Both the UK and the US have a simple scheme for higher powers of 1000 using Latin Numeral Prefixes (LNP) as follows:

UK LNP-illion = $(\text{million})^{LNP}$
US LNP-illion = $(\text{thousand}) \times (\text{thousand})^{LNP}$

and so:

	UK	US	
10^6	million	million	Mega
10^9	milliard	billion	Giga
10^{12}	billion	trillion	Tera
10^{15}	thousand billion	quadrillion	
10^{18}	trillion	quintillion	
10^{21}	thousand trillion	sextillion	
10^{24}	quadrillion	septillion	
	and so on		

The decimal point is written raised (·79) in England, rather than as a period, and is pronounced point seven nine, not point seven T nine. Where the UK and the US use a comma, most of Europe uses a space. No doubt a literal translation of our "floating point" is as amusing to the Germans as the literal translation of their "showing comma" is to us.

Michael J Cook
1658 S Stelling
Cupertino CA 95014

TWO TIPS FROM TEXAS

To answer part of Jan Kok's question in the September 1977 BYTE (page 179). According to the *Oxford English Dictionary,* billion was created in the 16th century as the second power of million:

$$10^{6^2} = 10^{12}$$

Similarly trillion was the third power and quadrillion the fourth. (May I speculate that the need arose from inflation and expansion?) The *OED* also stated that French arithmeticians changed the usage of the words (presumably in the development of the metric system) to indicate the number of thousands rather than millions. American usage probably arose when we adopted the metric system for money, though we never got around to adopting (until now) the rest of the system.

I can not find a specific reference to the European usage of the comma where we use the point, but I wouldn't be surprised to learn it was adopted by the French with the metric system, partly to be different and partly based on different use of punctuation in French.

I would also like to suggest an answer to Ira Rampil's request for an alternative cutting device for Slit-N-Wrap. I use a pair of small blunt nosed scissors (Revlon 2051) which are sold for clipping hairs from ears and noses without damage. The broadened ends mean the tips are stiff, and do not twist around the wire and will not scrape the circuit board.

Mike Firth
104 N St Mary
Dallas TX 75214

SR-52 AND PR-100 EXPERIMENTS

Webb Simmons in September 1977 BYTE (page 176) discovered that the Texas Instruments SR-51 calculator can be coupled to a PR-100A to provide printout capability. I have obtained similar results when I used my SR-51A. Unhappily, a more recent version of the SR-51, (the SR-51-11), cannot be connected to the PC-100A because of a redesign of the battery compartment. Although the SR-50A has a print cradle connector similar to the SR-51, and fits on the printer, apparently it is not preprogrammed for printout.

Incidentally, the "other" position of the PC-100A 3-position switch is for the new TI-58 and TI-59 programmable calculators.

Ralph Mednick
6 Hopkins Rd
Peabody MA 01960

SR-52 AND PR-100 EXPERIMENTS, CONTINUED

I read with interest the letter from Webb Simmons in the September 1977 BYTE (page 176) concerning use of the Texas Instruments SR-51 with the PC-100A printer. I connected my SR-51 to the printer after selecting the SR-52 mode as Webb indicated. The print mode worked fine but I never could get the trace mode to work. Every time I selected the trace mode I got a "1" and a "?" on my printout. The trace mode works fine with my TI 59 calculator so I know there is nothing wrong with the printer. Perhaps all SR-51s are not the same. I would be interested to hear what luck other readers have had with this experiment.

Carl Oehmann
9048 Posada Way
Sacramento CA 95826

MORE ON SR-51 AND PC-100A COMBOS

I wish to thank you and Webb Simmons (September 1977 BYTE, page 176) for the note, "More Hidden Gold: PC-100A Operates with SR-51."

In fact, the Texas Instruments' PC-100A also works perfectly well with the SR-51A hand calculator in exactly the same way as does the SR-51.

However, the SR-51-II does not have the 12 pad connector strip, so that it is not possible to obtain hard copy from a PC-100A and SR-51-II combination. This development seems to make used (but in good condition) SR-51 and SR-51A model calculators desirable items.

One must also note that the new Hewlett-Packard HP-10 seems to be designed to fill the same needs as an SR-51 and PC-100A combination.

Around our laboratory there are four SR-51As and one SR-51; the proud owners of these calculators now want some PC-100As. (They will probably pool resources to get one.)

I wonder, however, if the SR-50 and SR-40 were also designed to fit a PC-100A?

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CANADA

SIMULATING ONESELF?

I just received the October 1977 issue of BYTE, and I was reading an article by Mr Chung entitled "An 8080 Simulator" (page 70). It is on this article that I wish to comment.

While there are clearly useful applications for simulators that allow the execution (or interpretation) of assembly (or even machine) language programs of some machine on a different machine, it escapes me why one would want to emulate one machine's instruction set *on itself*. An apparent exception is the tester and debugger presented in the article. It appears that by interpreting each instruction individually it is possible to discontinue execution of the program at any point, called a breakpoint. A break may occur because the user wished to discontinue execution when certain conditions were satisfied, or even each time execution passed some address in the program. Both are obviously extremely useful when debugging. Upon detecting a break, the debugger presumably could enter a command mode where the user could examine and change memory locations and registers. Eventually execution could be resumed through some command, at which point the debugger would start interpreting the instructions again, watching for breakpoints. All very useful, but very slow. Each instruction is interpreted by the debugger, and consequently the debugged program's execution time might well be increased by several orders of magnitude.

I would like to propose a much more efficient method for implementing the same facility. Readers familiar with the DECsystem-10 debugger DDT will recognize the technique I am about to present. It hinges on the following

simple concept: Replace the instruction in the breakpoint address with a subroutine call instruction. (I am not familiar with the 8080 instruction set so I am not able to give a particular instruction, although I do not doubt that one exists.) This call would be to a routine in the debugger! The rest is easy. The routine saves the program registers, restores debugger registers (saved earlier) and dispatches to the command interpreter routine. This routine must be clever in two respects: first, if the user attempts to examine a breakpointed location, this must be detected. This is so that the original instruction may be displayed. Of course the breakpointed location will still contain the "call" instruction, which is not what the user wants to see. (By the same token, if he wants to modify the breakpointed location, we must modify the saved breakpoint instruction [in a breakpoint instruction table somewhere], not the actual instruction in the breakpointed location, which of course will hold the "call" that caused the breakpoint to begin with.) Secondly, when the user resumes the execution of the program, the debugger must first (individually) execute the saved breakpoint instruction (remember to first restore registers) before returning to the main code.

If my presentation was lucid, it should be clear that this technique is quite a lot more efficient than Mr Chung's method of interpreting each instruction. It will execute the program at *processor speed*, up to the breakpoint.

I read your journal with great interest and enjoy it immensely. I hope that this contribution will be of use to your readers and add to the excellence of BYTE.

Ralph Salas
29C Wycoma Way
Waltham MA 02154

Use of the 8080 simulator is an excellent way to trace the operations of a program, in a mode which depends on human responses rather than on absolute speed. It is thus not clear that the floating breakpoint technique would be the best method to employ. (I coin the term "floating breakpoint" to describe the act of setting a breakpoint, then restoring original code at the breakpoint while inserting a new breakpoint after the next instruction in sequence. An article by Robert Grappel and Jack Hemenway in the December 1977 BYTE (see "Jack And The Machine Debug" page 91) goes into the general design of such a floating breakpoint method of single step execution and tracing. Where tracing or debugging of read only memory software is involved, the simulator technique is the only one which will work, since breakpoints can not be set in read only memory.

In a recent phone call, Chuck Adams at Texas A & M University reported that the 8080 simulator by Kin-man Chung proved an excellent tool in the understanding of some otherwise undocumented software he was looking at.

COMMENTS ON WALSH FUNCTIONS

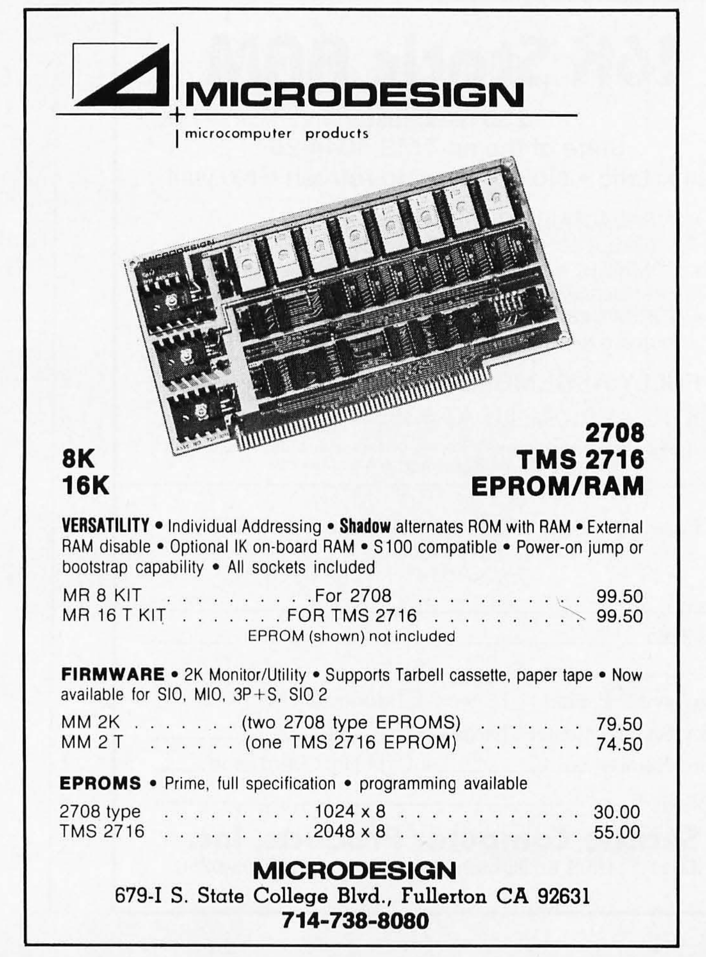
It was interesting to see the article on Walsh functions by B F Jacoby appearing in your September 1977 issue (page 190). The application of Walsh functions was a very active field about five years ago, but interest has dropped off since then mainly because advances in digital circuits have made it possible to use digital circuits in the Fourier domain. However, it is still very useful for designers to know about Walsh functions because they offer excellent solutions to many design problems. In the past couple of years we have seen several waveshaping circuits that actually used Walsh functions although the designers apparently had developed the circuits by trial and error. The material in your article would have led them quickly to the solution.

The mention of my own work applying Walsh functions to electronic music synthesis has brought in several inquiries. The use of Walsh functions for this purpose was first suggested to me by Dr Carl Frederick in 1972. A summary of my work can be found in *Journal of the Audio Engineering Society*, volume 21, number 8 (October 1973), and in volume 23, number 7 (September 1975), as well as in our own *Electronotes* publications. At about the same time, Hal Chamberlin was doing a comparative study of Walsh and Fourier synthesis and we published this report. To my knowledge, there are probably only a few music synthesis projects using Walsh functions still under investigation, although quite a few are still in use.

Any reader looking for more information on Walsh functions can find additional references listed in my papers mentioned above, or they may write to us for any special needs since we have lists containing hundreds of references.

Bernie Hutchins, editor
Electronotes
1 Pleasant Ln
Ithaca NY 14850

Walsh functions are far from dead, however. For example, the IEEE Transactions on Computers *has a table of contents category "Walsh Transforms" which is represented by one paper in the August 1977 issue (volume C-26, number 8). For electronic music, however, the need of weighted resistors makes them more complicated as a design element than a number of simpler techniques.* ■



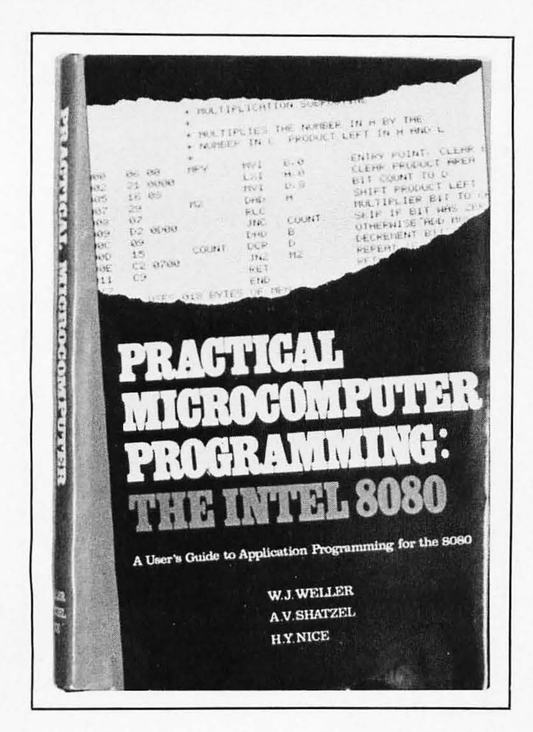
Book Reviews

Practical Microcomputer Programming: the Intel 8080 *by W J Weller, A V Shatzel and H Y Nice, Northern Technology Books, 1976, $23.95.*

This is the first text on 8080 assembler programming which I have run across, and as such is a welcome supplement to (or replacement for) previous books on the subject. The new book is an introduction to 8080 assembler written for beginners; beginners here meaning those who do not know any assembler language. The book would be very hard going for someone who did not know BASIC, FORTRAN, or some other higher level language; the authors assume familiarity with loops, subroutines and programming in general. Most of the sample programs in the book could be used on any 8080 machine; some of the IO and interrupt sections are machine dependent. The authors use an Altair and a minicomputer based cross assembler.

The first three chapters introduce binary arithmetic, logical operations and the basic structure of the computer. This section concludes with an introduction to the concept of programming and what an assembler does. The next few chapters concentrate on the most common tasks faced by the programmer: moving data, memory addressing modes, binary arithmetic and logical operations. The third logical segment (CSECT?) concerns the use of the stack, of subroutines, and of tables and arrays. Next the authors describe and illustrate simple and complex IO, conversion between binary and other ways of representing data (decimal, BCD, hexadecimal, ASCII), and graphical representation. The latter is contained in the complex IO chapter where a dot matrix printer is made to print in the Russian alphabet using "RUSKII" (Russian Unified Standard Key for Information Interchange, an invention of the authors). Decimal arithmetic and digital to analog conversions are then taken up, and the final two chapters proper are devoted to interrupts. There is a final chapter on debugging, and then appendices which give source and object code for the debugger, a loader, the cross assembler, and a table used to produce the Russian alphabet.

Generally I found the book excellent. I was only able to find a couple of relatively trivial typos (on page 153 RAR should be RAL, and on page 182 OSVCE should be



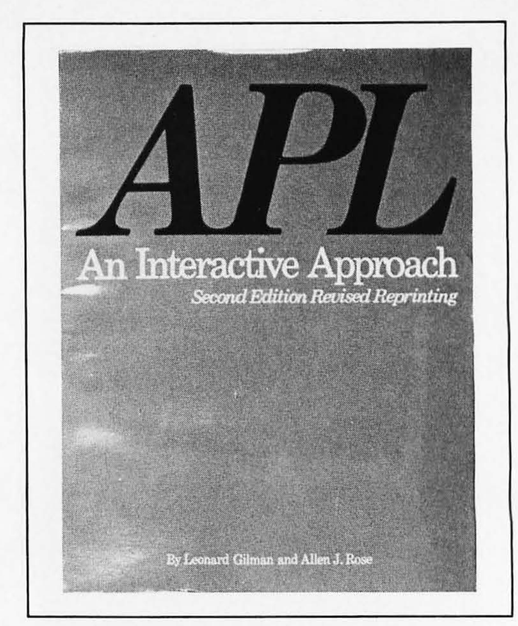
CSVCE), and the illustrations were very good. I would have liked to have seen a section on floating point arithmetic, and it would have helped to give a table of the instruction set somewhere, but the authors must presume this is available elsewhere.

John A Lehman
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Ann Arbor MI 48103■

APL An Interactive Approach, second edition, *by Leonard Gilman and Allen Rose, John Wiley & Sons, Inc, New York, 1974, 384 pp, $11.95 (paperback).*

An important element in the title of this book is "interactive." APL, A Programming Language, is indeed interactive. Throughout the book this feature is not only accented; it is capitalized upon. One does not merely read the book. A budding APL programmer can either interact with an APL workspace that has been preprogrammed to track the book or, when this is not practical, he or she can interact with the computer surrogate found interwoven into the text in the form of a listing which includes both human input and computer response.

APL An Interactive Approach gives an understandable presentation of APL operators (also called APL functions), user programs (called defined functions), workspace management, and information which can best be described as "advanced topics." Although these "advanced topics" might not be implemented on home microcomputer APL systems of the near future, the



adage that too much is better than too little seems pertinent.

The general tone of the book is technique and, as could be expected, the type of technique emphasized is the use of APL functions. (Branching is not discussed until halfway through the book. However, the authors have chosen to stress the alternatives to branching which APL provides in order to combat what must be a natural tendency to branch.) Technique is but one course and, "One course neither a meal nor a graduate makes!" I believe that additional emphasis is needed on program (function) organization, the use of functions as subroutines, debugging, and error correction. An additional appendix on "error messages, their causes and corrections" and an expanded appendix on "APL functions," both comprehensive enough to be used as stand alone work aids, would have been helpful.

A revised printing of the second edition has been released recently, the major change being an easier to read type style. Information relating to the use of the IBM 5100 portable computer was also included.

Is this book for you? Assuming you have a strong desire for information concerning APL, I would say, "Yes." If your interest is casual and you expect programming languages to be more conversational than `→BOOKSTORE×ι(DESIRE>NIL)∨NEED='YES'` then my answer would not be so unequivocal. (Note: → can be read as "GOTO" and ×ι as "IF;" I leave the rest to you!)

Thomas E Hoge
41 Fern St
Rocky Hill CT 06067■

Clubs and Newsletters

Conducted by
David Wozmak

SOL User's Society

On a hot Sunday afternoon, about 30 owners of Processor Technology SOL computers gathered in a Stanford University auditorium to organize the SOL Users' Society (SOLUS). The meeting was arranged by Bill Burns, Ron Findlay, Dave Fylstra, and Ben Milander, who had been conducting preliminary SOL users' meetings at the Homebrew Computer Club. As the SOLUS steering committee, these four men discussed the goals, structure, and functions of SOLUS.

It was decided that SOLUS will have a cooperative but independent relationship with Processor Technology. The goals of the society are: to facilitate communication among SOL users and to provide a mechansim for exchange of SOL compatible hardware and software products by independent sources. Membership is open to owners of SOL computers or of other computers configured like the SOL. The Society is primarily a personal computer users' group, although a commercial interest group may be formed within SOLUS.

The item above is from Stan Sokolow, the editor of *SOLUS News.* To get in touch with SOLUS, write to Stan Sokolow, 1690 Woodside Rd #219, Redwood City CA 94061.

The International Classified Advertiser for Computer Hobbyists (Bitbucket)

Bitbucket is published twice a month and sent via first class mail. Computerfest announcements, club meeting schedules, interclub requests, and news articles (flea markets, special events, etc) are published free of charge. *Bitbucket* is mailed free to all clubs. To send for more information, write *Bitbucket,* M C Corporation, publisher, POB 314, Libertyville IL 60048.

SR-52 Users' Club

Here's a club for owners and users of Texas Instruments programmable calcu-

lators. Membership is open to anyone. The club is neither sponsored by nor officially sanctioned by Texas Instruments. To date there are over 700 members. The club publishes a newsletter, *52 Notes,* which contains programs, routines, and various other information. Write to R C Vanderburgh, 9459 Taylorsville Rd, Dayton OH 45424.

RICH

The Rhode Island Computer Hobbyists hold meetings on the third Tuesday of every month. Upcoming meetings will feature presentations of solar energy projects, the new Heath line, and terminals for the deaf, to mention a few. The new NET message service allows anyone with a terminal and a modem to dial a club computer to get news and receive or leave messages. Contact the Rhode Island Computer Hobbyists, POB 599, Bristol RI 02809.

Lincoln NE Computer Club

Computer hobbyists in the Lincoln NE area are invited to join the Lincoln Computer Club. The club was formed in early 1977, and has been meeting monthly ever since. Meetings are held the first Wednesday of each month at 7 PM at the South Branch Library at 27th Av and South St. For further information contact Hubert O Paulson Jr, 422 Dale Dr, Lincoln NE 68510.

Computer Amateurs of South Jersey

A new club, the Computer Amateurs of South Jersey, invite the participation of all interested parties, both novices and professionals. User groups have been formed for the 6800, 6502 and the 8080 processors. Meetings are held at 7:30 PM on the last Tuesday of each month at the National Park Municipal Building, 7 S Grove Av, National Park NJ. For additional information please call (609) 541-8296 or write Charles Knott, 3088 Congress Rd, Camden NJ 08104.

Tidewater VA Computer Club

This club, located in the tidewater area of Virginia (Norfolk, Virginia Beach, Chesapeake, Portsmouth) has a membership of about 100. Club meetings are held in the Electronics Computer Programming Institute, Janaf Office Building, Janaf Shopping Center in Norfolk at 7:30 PM on the first and third Tuesdays of each month. Contact C Dawson Yeomans, 677 Lord Dunmore Dr, Virginia Beach VA 23462.

Electronotes

This is the newsletter of the Musical Engineering Group. Bernie Hutchins has been publishing this unique and valuable newsletter since the early 1970s. It contains technical material pertaining to electronic music and related subjects. There are 20 to 25 pages in every issue, all of them informative. To submit articles or to subscribe, write to B A Hutchins, 1 Pleasant Ln, Ithaca NY 14850.

Calculator Lib

There exists in Oxnard CA a man named Gene Hegedux who edits a newsletter called *Calculator Lib*. This publication is devoted to the spreading of information and ideas about calculators. In it are various tricks, hidden secrets and humorous items about calculators (not just programmable calculators, either). To subscribe contact Gene Hegedus, POB 2151, Oxnard CA 93034.

Alamo Computer Enthusiasts

ACE is a group of microcomputer enthusiasts in the San Antonio TX area who have gotten together to publish a newsletter. The club meets on the fourth Friday of each month at 7:30 PM in room 104, Chapman Graduate Center, Trinity University. Contact John Stanton, 7517 Jonquill, San Antonio TX 78233.

Southern Illinois Computing Association

The Southern Illinois Computing Association (SICA) draws its members from the academic, business, professional and hobbyist fields. The organization meets the first Monday of the month at Southern Illinois University, Carbondale IL. For further information and a current copy of the organization's newsletter, contact James E Honey, SIU General Stores, Carbondale IL 62901.

Computer Hobbyist Group of North Texas

This group, led by Neil Ferguson, president, and Bill Lewis, vice president, is located in the Dallas area. It is an informal club in which people display their systems, exchange information, and so on. Their newsletter, *The Printed Circuit*, looks good and contains vital club information, classifieds, and coming events. If you want to become a member, or get more information, contact Neil Ferguson, POB 1344, Grand Prairie TX 75051. ■

Continued from page 6

executed (or shall I say, "understood"?) by the computer system. When we figure out what it is that we want to get done, then the process of automating that intention reduces to a purely mechanical procedure.

The amplification of our thoughts represented by a computer's operation comes in several ways. The computer can automate and execute procedures orders of magnitude faster than a human brain can operate; a computer can record procedures in some form of storage, for recall at the direction of its user; by requiring explicit and consistent instructions, a computer acts as a tireless crusader for consistency and accuracy in our knowledge of innumerable subjects. Ralph Waldo Emerson commented that ". . .a foolish consistency is the hobgoblin of little minds, adored by little statesmen and philosophers and divines." With the aid of these new mental amplifiers, we might add computers to the list of "little minds."

As a mental amplifier, the computer is perhaps the "ultimate tool" of our tool making species. Recognizing the nature of the computer as such a tool helps one to understand the multiple facets of personal computing. The general-purpose computer system is not confined by design to any particular application; its generality is the secret of its enthusiasm with users. Computers are indeed used in dedicated applications, and with great success, as evidenced by the newest crop of complicated video game machines, computer controlled sewing machines, and computer controlled automotive systems. But in such dedicated applications, we merely use the results of the amplified thoughts of the designer of the application system, and if those thoughts disagree with our own thoughts on the way the system should work, then there is little prospect for improvement or customization of the application. The general-purpose computer in contrast is oriented toward an interactive user who needs the mental amplification process in an individualized context. The key to such computers' enthusiastic reception as "personal computers" is this flexibility which is present in the user who knows how to program with the tools available and can proceed to create an application or modify a canned application to fit a custom situation.

Think of an analogy to the piano or any other musical instrument which requires some skill to play. As an avocational pianist, I buy a "stock" program for an "appli-

cation" of the piano, for example a Scott Joplin piano rag, a Waldteufel salon style Viennese waltz, or a piano sonata by Beethoven. I do not pretend to be an original "programmer" of the music, so I purchase the printed form of these works and proceed to play them in my own imperfect style, customized as it were to my own characteristics as a piano player. (I can buy completely canned music, too, in the form of mass produced record albums of famous artists which are musically the equivalent of game programs purchased for specific games machines and written by the games' artists.) The piano is my general-purpose musical instrument which can be adapted to any one of a wide diversity of musical styles and emotional states. In a like manner, the personal computer as a general-purpose computer is not confined to any one mode of operation — it merely provides a mechanism for implementation.

The users of the personal computer in the past have tended to be those individuals who have most to gain from this personal thought amplifier, namely individuals involved in personal endeavors which can benefit from the automation of thoughts. Since everyone thinks to a greater or lesser degree, the market for personal computer equipment may in principle be limited only by the size of the human population; but for the near term it is those individuals who are involved with intellectual processes from art to business who benefit most from the small computer. The art of computer programming is a skill which I view as essential, in the same way that the art of driving is required to take advantage of the mobility of the automobile. Not everyone need be the programming equivalent of a skilled race or rally driver, but for people now growing up with programmable computers readily available, a programming skill analogous to the ordinary person's automobile driving skills is required. Anyone who would think otherwise is ignoring the essence of what makes the personal computer personal.

So, then, what does it really mean to have a personal computer? At an emotional level, it enhances one's understanding and thought processes through the ability to perform simulations and experiments; it gives one the opportunity to experience a joy of creation and practical benefits at whatever level programming is done. It gives its user a tool for understanding and interacting with the world which was not previously available and which enhances the human thought processes by allowing simple automation of well-defined operations. The total feedback in both spiritual and material benefits can be enormous.■

Simulation of Motion Part 3:

Model Rockets and Other Flying Objects

Stephen P Smith
POB 841
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Since becoming involved in personal computing, I've only met a few real applications oriented users. Most microcomputer owners are either hardware oriented, eg: hams or other electronics hobbyists, or they are software hackers. Both groups tend to love their machines for their own sake and not necessarily because they are useful. The users I've met who are more interested in the answers they get than in how they got them have all been running financial programs. Despite this thin showing, I believe that the next large group to "discover" personal computing is going to be applications oriented. They will be the business people and hobbyists who need more computing power than is available in a pocket calculator, but who can't justify access to a large computer.

Among this group will be the model rocket and aircraft builders. Those people delight in creating miniature NASAs, but they have always lacked one important resource, computing power. The government and the aerospace industry invest a great deal of effort in simulating flights long before any hardware is put together. Few hobbyists could do this until now. In this article, I'll show how a microcomputer can be used to simulate the flights of model or amateur rockets and aircraft. The simulations can be used as aids in design and "mission" planning. I also hope to demonstrate the desirability of personal computing as an adjunct to other pastimes.

As in my previous articles, these simulations are intended to serve as examples. The techniques involved can be applied in almost any real world application. The *lunar lander* game, for example, served to illustrate how simulations are separated into degrees of freedom, and how speed and position are predicted for steps into the future. Those concepts were also applied when we simulated the motion of an automobile suspension system. That simulation illustrated how forces could depend directly on the motion being simulated. It also served to introduce some powerful numerical techniques. All of these concepts will apply to the flight simulations. In addition, I'll show how to calculate the effects of a force which acts in two degrees of freedom at the same time. I'll also introduce angular motion and demonstrate the way in which a simulation keeps track of how fast a body is turning and where it is pointing. While developing a flight simulation in detail, I'll try to point out specific areas where these new techniques can be applied to the earlier applications.

Let's begin, in fact, by outlining a game

Body	C_d
flat plate (1 square meter)	0.7
sphere (0.1 meter diameter)	0.003
airplane body (2 square meters)	0.08
wing or fin edgewise (1 square meter)	0.012
model rocket (2 cm diameter)	0.0001
automobile (2 square meters)	0.6
motorcycle and rider (2/3 square meters)	0.25

Table 1: Drag coefficients for various bodies. These coefficients include the body area and air density term (1/2 x 1.192 kg/m^3). They are intended to be used in an equation of the form:

$$DRAG = SPEED^2 \times C_d$$

If larger or smaller bodies are used, a simple ratio of areas will convert the coefficient.

simulation you can program. In the lunar lander game, aerodynamic forces were neglected, but these forces must be considered for atmospheric flight. They also present a good example of forces which act in more than one degree of freedom. We will investigate them through the use of a simple game I'll call EVEL. The object of the game is to select the ramp angle and speed with which to leap a motorcycle over a given number of cards and land successfully on the downward ramp. The motion will be in two degrees of freedom, vertical and horizontal. The forces will be gravity and aerodynamic drag.

We have seen in the previous articles how gravity affects speed, and most people have an intuitive understanding of drag. Drag is the force you feel when you hold your hand out the window of a moving car. It is the resistance of air to a body moving through it and it acts directly opposite the motion. Drag is calculated in much the same way as the force created by an automobile shock absorber. In that example the force was equal to the speed multiplied by a damping coefficient. To calculate drag, we will multiply the speed squared by a constant called the drag coefficient (symbolically C_d). Drag coefficients for some common bodies are given in table 1. C_d takes into account the size, shape and surface texture of the body. In our simulations, it will also include a factor for the density of the air (1.19 kg per cubic meter). More detailed simulations will take into account the changes in air density and temperature which occur at higher altitudes and adjust the aerodynamic forces accordingly. To avoid this complication, we will restrict our simulations to altitudes within a few thousand meters of sea level. The formula we will use for calculating drag is $DRAG = SPEED^2 \times C_d$.

If the only motion is upward, the drag acts only in the vertical degree of freedom. There are also cases in which it acts only horizontally; but in general, there will be motion in both directions, and the drag, which acts directly opposite the motion, will be felt in both degrees of freedom. Because of its dependence on the square of the speed, we cannot calculate separate vertical and horizontal drags. We must calculate one force and apportion it between the two degrees of freedom.

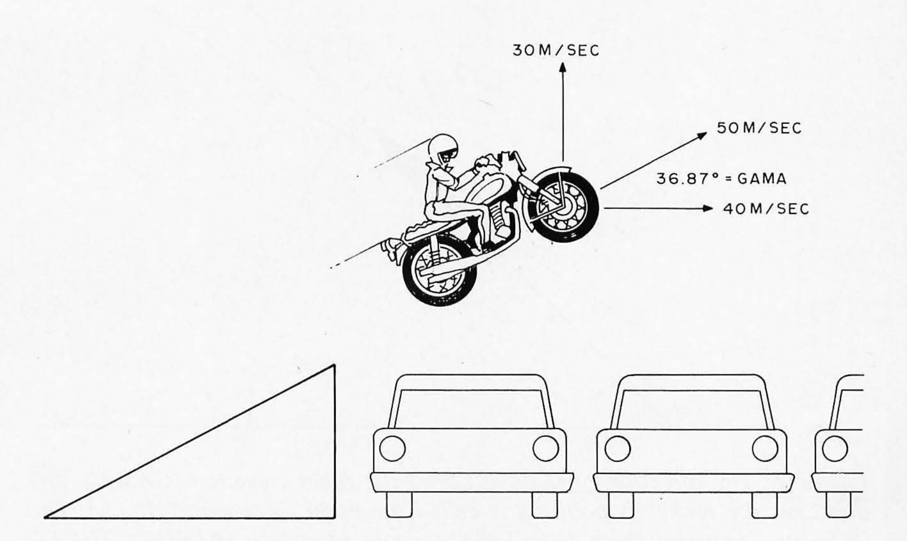


Figure 1: The total speed and flight elevation angle can be calculated from the horizontal and vertical speed components.

Figure 1 shows a typical case. Here a daredevil motorcyclist has just left his takeoff ramp. Suppose we know from a previous simulation step that his vertical speed is 30 meters per second (m/sec) and his horizontal speed is 40 m/sec. To calculate drag, we must first find the total speed. Our fortunate selection of degrees of freedom now becomes apparent, because the vertical and horizontal velocities can be seen to form two sides of a right triangle. We can compute the third side, or hypotenuse, by applying the theorem of Pythagoras ($C^2 = A^2 + B^2$). The total velocity will be equal to the square root of the sum of the squares of the speeds in each degree of freedom. In this case, the daredevil is moving at $\sqrt{30^2 + 40^2} = 50$ m/sec. Using C_d from table 1, we calculate a drag of $0.25 \times 50^2 = 625$ newtons, acting at some angle between horizontal and vertical. This angle is called the flight elevation (symbolically GAMA in some computer programs). It can be found using a little trigonometry. If we let horizontal be 0 degrees, and let vertical be 90 degrees, then GAMA is equal to the arc tangent of the vertical divided by horizontal velocity. In this case, GAMA = arc tan (30/40) = 36.87 degrees. Knowing the angle, it is easy to apportion the drag. The forces which result are called components of drag. The vertical component (symbolically D_v is given by $D_v = DRAG \times SIN (GAMA)$. The horizontal component, D_h, is given by $D_h = DRAG \times COS (GAMA)$. In

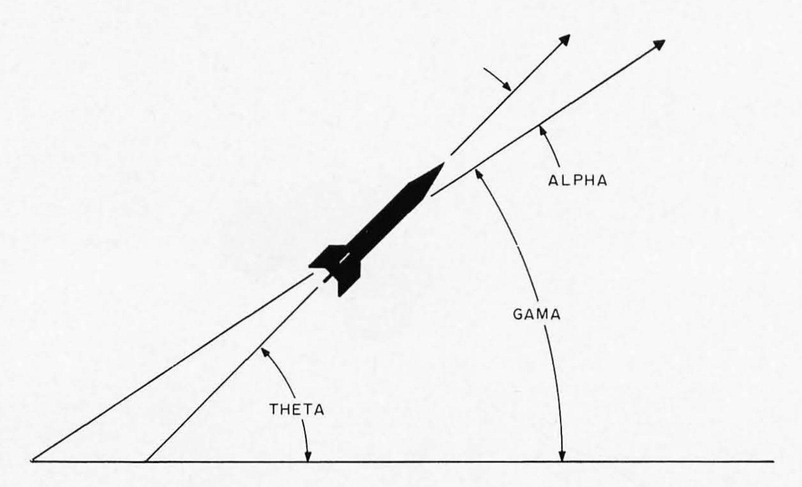


Figure 2: The direction of flight is called the flight elevation (GAMA). The direction the rocket is pointing is called the body elevation (THETA). The difference between them is called the angle of attack (ALPHA= THETA -GAMA).

the current example, $D_v = 625 \times SIN(36.87) = 375$ newtons, and $D_h = 625 \times COS(36.87) = 500$ newtons. You can check these calculations by noting that $\sqrt{375^2 + 500^2} = 625$. Readers familiar with trigonometry will be able to confirm that

$$DRAG = \sqrt{D_v^2 + D_h^2}$$

in every case. This is the same formula we used to find the total speed, so it should not be surprising to find that the vertical and horizontal speeds are also referred to as components.

The effect that the components of drag have on the components of speed depends, of course, on the mass. If our daredevil is fairly small, and rides a light motorcycle, the total mass in flight might be 150 kg. During a step of 0.1 seconds, the horizontal speed will decrease by 500/150x0.1 = 0.333 m/sec. A similar change occurs in the vertical speed, but there we must also include gravity. Remember from the previous simulations that each second, gravity subtracts 9.8 m/sec from the vertical speed. In 0.1 seconds it will change from 30 m/sec to 30−(375/150 + 9.8)x0.1 = 28.77 m/sec. Knowing the new speeds, you can compute the new position, the new drag and the new flight elevation. The simulation can be stepped forward again and again until the daredevil returns to earth.

Part 1 of this series, "An Improved Lunar Lander Algorithm," began on page 18 of November 1977 BYTE, while part 2, "An Automobile Suspension," appeared on page 112 of December 1977.

Because the drag components depend on the square of the speed, it will probably be necessary to use the predictor-corrector formulas from my previous article to obtain realistic results. The initial conditions of total speed and ramp angle must be chosen. For the first simulation step set GAMA equal to the ramp angle and let the vertical speed component equal SPEEDxSIN (GAMA) and the horizontal component equal SPEEDxCOS (GAMA). Figure that a car is about 6 meters long, a bus about 15 meters, and the Snake River Canyon is 1451 meters wide. Good luck.

In many respects, a rocket or aircraft in flight is much like our daredevil. It will be moving horizontally and vertically and will be acted upon by gravity and drag. There are some other forces to be considered, however. For example, early in a rocket's flight, its engine will be producing thrust. Unless the rocket is pointing directly upward or directly parallel to the ground, we will also have to apportion this force between horizontal and vertical directions.

One way to do this is to assume that the rocket always points in exactly the direction it is moving. The flight elevation angle, GAMA, can then be used to apportion thrust just as it was used for drag. At each simulation step, the program can interpolate a table to find the value of thrust corresponding to the current time. It then computes the components and applies them to predict new speeds and position. In this manner we can build a two degree of freedom rocket trajectory simulation. This simulation might also be used for a game. Set up a duel between two artillery battalions, or better still, program a real time simulation like the lunar lander game of my first article and try to hit a moving target.

For most flight vehicles, the tendency to point in the direction of movement is a desirable characteristic. Unfortunately, this is not generally the case. Vehicle imperfections, the effect of wind, and just the fact that it takes a finite amount of time to turn the vehicle, all affect the pointing of a rocket. In order to indicate where the rocket is pointing, we define another angle, the body elevation angle (symbolically THETA). THETA tells us where the vehicle is pointed and is used to apportion thrust. The difference between THETA and GAMA is called the angle of attack (symbolically ALPHA). It is illustrated in figure 2.

Unlike GAMA, there are no components which may be used to compute THETA. We must keep track of it with a third degree of freedom. Just as altitude is calculated as the position in the vertical degree of freedom, THETA may be calculated as the position in this third, or angular, degree of freedom.

Angular motion is handled in exactly the same way as the linear motions we have already been simulating. Just as position has its angular equivalent, so do speed, force and mass. It is as easy to calculate the speed with which a body turns as it is to find the speed with which it falls.

First we must calculate the angular equivalent of a force. These are called moments (also called "torque"), and have metric units of newton meters. As the units imply, each moment has a force as part of its definition, but it also depends on how much leverage the force has. For example, suppose you apply a force of 10 newtons to the end of a 15 cm (0.15 meter) wrench. A moment of $10 \times 0.15 = 1.5$ newton meters will be transferred to the bolt. If a 25 cm wrench were used, a moment of $10 \times 0.25 = 2.5$ newton meters would result, and the bolt would be proportionately tighter. In rocket flights a moment results as an aerodynamic effect whenever THETA is not equal to GAMA. It has its own coefficient, C_m. For small angles of attack, this coefficient is multiplied first by the square of the speed (linear speed, not angular) and then by the angle of attack (ALPHA=THETA-GAMA). The aerodynamic moment is therefore caused because the rocket is trying to point itself in the direction it is moving.

The next element to be considered in the angular equation is the equivalent of mass. This is called moment of inertia, and the leverage concept applies to it also. The moment of inertia (usually shown symbolically as an upper case I) depends on the mass of the body, and also how widely spaced the mass is. For example, a 50 kg set of bar bells would have a much larger moment of inertia than a single 50 kg weight. The units of I are kilogram meters. Like mass, moment of inertia is a property of matter. In our rocket simulation, both may change as fuel is burned, but their values can be determined at any given time. It is general practice to construct tables of mass and moment of inertia which parallel the thrust table we have already introduced. In each simulation step, our program will interpolate the table to find the current value of moment of inertia and use it to find the effect of the moments. The value of the metric units will now become apparent.

Just as the force in newtons was divided by the mass in kilograms to find exactly the

```
100 REM PITCH PLANE TRAJECTOTY SIMULATION
110 REM INITIALIZE VARIABLES
120 DATA 0,0,0,0,0,0,0,0,0,0,0,0,0
130 READ U,W,V,U1,W1,V2,X1,Z1,Q1,F1,M1,I1,K
140 REM INITIALIZE TIME(T),STEP SIZE(H), PRINT INTERVAL(K1)
150 H=0.01
160 LET T=0
170 LET T1=T
171 LET K1=0.1/H
180 REM SET INITIAL ALTITUDE (Z1>0)
190 LET Z1=1
200 REM SET DRAG(D) AND MOMENT(P) COEFFICIENTS
210 LET D=-1.0E-4
220 LET P=-3.0E-5
230 REM SET LAUNCHER LENGTH(R) AND ELEVATION(L)
240 L=90
250 PRINT "LAUNCH ELEVATION =";L;" DEGREES"
260 LET L=L*0.01745
270 LET L1=L
272 LET G=L
280 LET R=Z1+1
300 REM SET WIND SPEED
310 N=5
320 PRINT "WIND SPEED =";N;" METERS/SECOND"
330 LET U1=N
340 REM END INITIALIZATION, BEGIN TRAJECTORY
350 PRINT "TIME                    ALTITUDE      RANGE        SPEED"
360 PRINT "(SEC)                   (METERS)     (METERS)     (M/SEC)"
370 REM GET THRUST(F), MASS(M), & MOMENT OF INERTIA (I)"
380 GOSUB 950
390 LET T=T+H
400 LET K=K+1
410 REM PREDICTOR FORMULAS
415 REM B,W,Z,ARE VERTICAL ACCELERATION,SPEED & POSITION
420 LET B1=(SIN(G)*D*V2+SIN(L)*F)/M-9.8
430 LET W=W1+H*B1
440 LET Z=Z1+H*W1
460 REM A,U,X ARE HORIZONTAL ACCELERATION, SPEED & POSITION
470 LET A1=(COS(G)*D*V2+COS(L)*F)/M
480 LET U=U1+H*A1
490 LET X=X1+H*(U1-N)
500 LET V2=(U+N)↑2+W↑2
510 LET V=SQR(V2)
511 REM NO ANGULAR MOTION ON LAUNCHER
512 IF Z<R THEN 590
513 LET G=ATN(W/(U+N))
514 IF U+N>0 THEN 530
515 LET G=G+3.14159
520 REM NEGLCT ANGULAR MOTION AFTER BURNOUT
530 IF F=0 THEN 610
535 REM C,Q,L ARE ANGULAR ACCELERATION, SPEED & POSITION
540 LET C1=P*(L-G)*V2/I
550 LET Q=Q1+H*C1
560 LET L=L1+H*Q1
590 GOSUB 950
600 REM CORRECTOR FORMULAS
610 LET B=(SIN(G)*D*V2+SIN(L)*F)/M-9.8
620 LET W=W1+H/2*(B+B1)
630 LET Z=Z1+H/2*(W+W1)
640 LET W1=W
660 Z1=Z
680 LET A=(COS(G)*D*V2+COS(L)*L)/M
690 LET U=U1+H/2*(A+A1)
700 LET X=X1+H/2*(U+U1)
710 LET U1=U
720 LET X1=X
730 LET V2=(U+N)↑2+W↑2
740 LET V=SQR(V2)
750 REM NO ANGULAR MOTION ON LAUNCHER
751 IF Z<R THEN 880
752 G=ATN(W/(U+N))
753 IF U+N>0 THEN 770
754 G=G+3.14159
760 REM NEGLECT ANGULAR MOTION AFTER BURNOUT
770 IF F=0 THEN 880
780 LET C=P*(L-G)*V2/I
790 LET Q=Q1+H/2*(C+C1)
800 LET L=L1+H/2*(Q+Q1)
810 LET Q1=Q
820 LET L1=L
880 IF K<K1 THEN 390
890 PRINT T,Z,X,V
900 LET K=0
920 IF Z>0 THEN 390
930 REM STOP WHEN ALTITUDE RETURNS TO ZERO
940 STOP
950 REM INTERPOLATE TIME TABLE FOR F,M,& I
960 DAT 0,5.6,0.0458,1.1E-4,0.1,13.3,0.0446,1.1E-4,0.2,5.6,0.0434,1.1E-4
970 DATA 1.6,5.6,0.0337,1.0E-4,1.7,5.6,0.0333,1.0E-4,100,0,0.0333,1.0E-4
980 IF T<T1 THEN 1050
990 LET T2=T1
1000 LET F2=F1
1010 LET M2=M1
1020 LET I2=I1
1030 READ T1,F1,M1,I1
1040 GO TO 980
1050 LET H4=(T-T2)/(T1-T2)
1060 LET F=F2+(F1-F2)*H4
1070 LET M=M2+(M1-M2)*H4
1080 LET I=I2+(I1-I2)*H4
1090 RETURN
1100 END
```

A Model Rocket Simulator

Listing 1: This BASIC program illustrates the use of an angular degree of freedom to apportion a force between two linear degrees. It simulates the flight of a model rocket that might be built from widely available kits. During the early part of the flight (approximately 1 meter), the rocket rides on a guiding rod. The rod prevents the body from turning, so angular motion must be suppressed in the simulation. After leaving the launcher, the vertical, horizontal and angular pitching motions are all considered. A short time later, however, the fuel will be exhausted and the thrust will drop to zero. Because the only reason for computing THETA was to apportion the thrust, angular motion may be neglected from this point until the vertical position becomes zero (rocket returns to earth) and the simulation ends.

This type of simulation is particularly useful for determining the effect of wind on a rocket. The tendency a rocket has to point in the direction it is moving also causes it to turn into the wind. The highest altitude may not, therefore, be achieved with a vertical launch. By running a series of simulations on his/her personal computer, a model rocket builder can determine in advance the ideal launch angle for various steady state wind speeds. The plots shown in figure 3 illustrate this type of study. Note that in each case the horizontal degree of freedom is aligned with the wind.

Because the forces and moments in this simulation depend on the motion, the predictor-corrector method has been applied. To conserve space, however, it is not the fourth order method used in the automotive simulation of last month's article, but a shorter second order version. Improved accuracy would result if you were to implement the longer formulas. You may also want to customize the output. For example, a plot of angle of attack versus time might be interesting. To print out ALPHA in degrees, use (L-G) x 57.295 to convert from units of radians. Special output exactly at apogee (maximum altitude), impact, or motor burnout might also be helpful in evaluating performance. The code is well-commented, so feel free to dig in and adapt this program to your own needs.

change in speed each second, so the moment in newton meters can be divided by the moment of inertia in kilogram meters to find exactly the change in angular speed. In angular degrees of freedom the units of speed are radians per second and the position will be computed in radians. There are 2π radians in a full circle, so 1 radian equals 57.296 degrees. Because most BASIC interpreters perform trignometric calculations in radians, these units are to be preferred. Conversion to degrees is easily made for input and output.

Once the effect of each moment is known, it is multiplied by the time step size and added to the speed in exactly the same technique used for linear motion. Similarly the angular speed is multiplied by step size to update the angular position. The predictor-corrector method may be applied by saving moments, and speeds from previous steps. I have included a BASIC program with this article which involves both the predictor-corrector formula and angular motion in a three degree of freedom (pitch plane) trajectory simulation. Noting the similarity between the angular and linear equations used there should make this technique easier to understand.

The concept of angular motion is easily transferred to other applications, but to make best use of it you really need some familiarity with the forces and moments which may appear. For example, an automotive enthusiast will already understand how the road surface induces motion in the body of a car. We saw last month how to simulate that motion for one wheel. If you include two wheels, the front and back on one side, a second degree of freedom in body motion is introduced. Most people would recognize that, but only someone familiar with automobiles might realize immediately that the two ends of the body will not move up and down entirely independently. The second degree of freedom must be an angular one. It will measure the pitching motion of the car while the original degree measures its overall up and down motion. The forces created by each set of suspension parts will contribute to the linear motion, and will be multiplied by their leverage (perhaps their distance from the driver's seat) to determine their affect on the angular motion. At each step, the angular motion will be combined with the linear motion to compute new forces, moments, etc, and the procedure will begin again. Just how those angular motions are combined with the linear ones, and how the leverage of a force is determined, will be the subjects of the fourth and last article in this series.■

Figure 3: The program of listing 1 can be used to determine the best launcher elevation for any given wind.

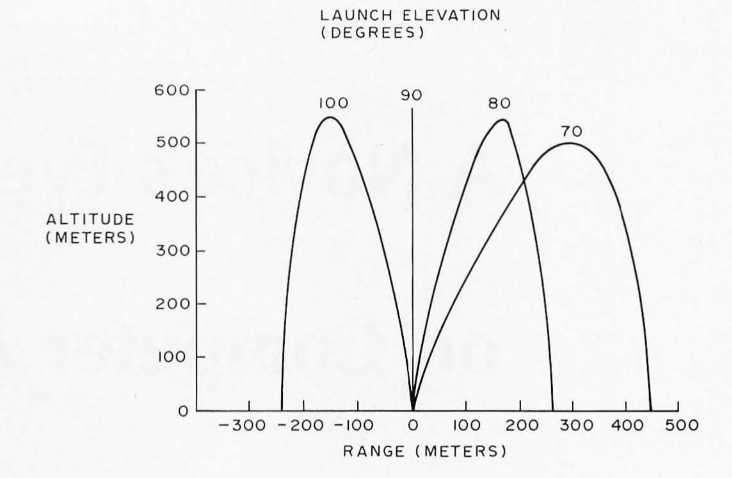


Figure 3a: Trajectories with no wind.

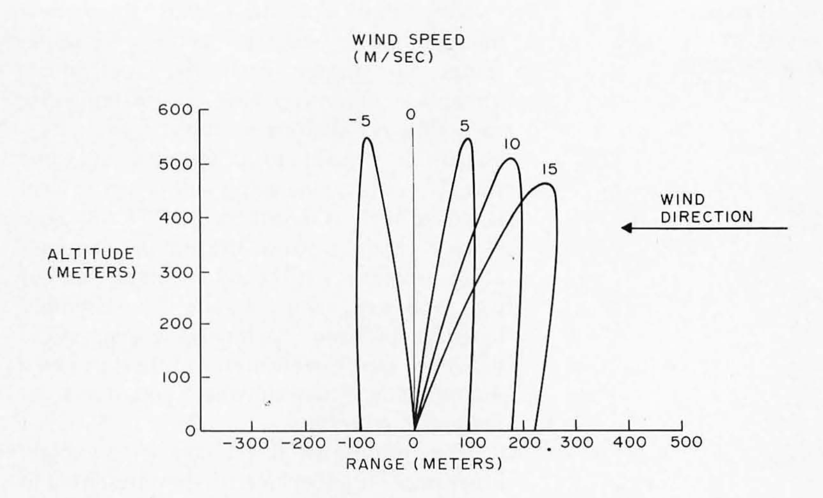


Figure 3b: 90° launch with wind.

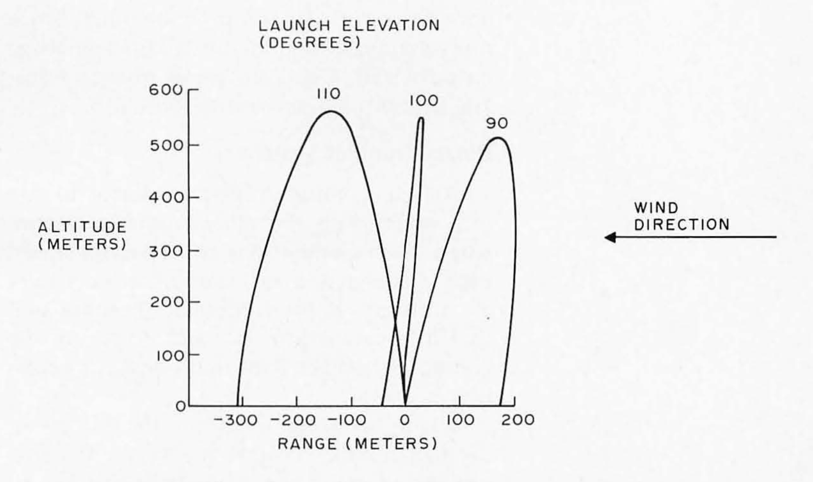


Figure 3c: Trajectories with 10 m/sec wind.

A Novice's Eye on Computer Arithmetic

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8 Overlook Dr
Medway MA 02053

Now that you have your shiny new microcomputer you want to use it for something. No matter what the application, someplace in it you have to use numbers: to count, do arithmetic, input from a keyboard, or output to a terminal of some sort. If you are operating with a higher level language such as BASIC or FORTRAN there is no problem since all the number manipulation programs are already included. Most of us, however, must work in assembly language or even machine language, and if you have never been there before it can be a discouraging situation when you don't get the expected results.

The purpose of this article is to explain how simple numbers are often represented in a computer and how to do the four basic arithmetic operations. Since the real world of people is decimal, not binary oriented, we have to convert from one to the other. Since most computer peripherals talk in a language called ASCII, I will also show how to translate that into binary and vice versa.

Binary Number System

All the computers you are liable to run into operate on the binary number system, where each element has two possible states, usually designated as 1 and 0. Let's consider an arbitrary 8 bit computer, meaning that the internal arithmetic and logic of the computer handles data that consists of eight bits at a time.

When counting in either the binary or decimal number system the first number is designated by 0 and the second number by 1. We run into difficulties when we try to express the number 2. In the decimal number system it is easy, 2. In the binary number system we have already used up the two allowable states with the first two numbers. What we need is an additional bit of information. When this bit is added we can now designate the number 2 by 10. This extra digit on the left represents a weight of $2^1 = 2$. (The rightmost digit has a weight of $2^0 = 1$.)

Each digit position in a number is assigned a weight dependent on where in the number it occurs. To obtain these weights take the base number and raise it to a power equal to the position of the digit in the number. The rightmost digit is the least significant digit and has the position index of zero. Following these two rules the weights for the decimal number system are: $10^0 = 1$, $10^1 = 10$, $10^2 = 100$, etc. In the binary number system the base number is 2 instead of 10. Substituting, we have the following weights: $2^0 = 1$, $2^1 = 2$, $2^2 = 4$, etc.

To translate a binary number into a decimal number just add up the weights of the digits which are 1s. Table 1 shows how the decimal numbers from 0 through 16 are written in binary and two other forms of numbering common in computers: hexadecimal, which uses a base of 16, and octal, which uses a base of 8.

The octal and hexadecimal forms are used to save you from writing out long strings of 1s and 0s which are hard to read and give plenty of opportunity for mistakes. For hexadecimal notation six new digit value graphics are needed to allow a total of 16 different digits, representing four bits. To fill this need the letters of the

Decimal Number	Binary Number					Hexadecimal		Octal	
	Weights = 16	8	4	2	1	Weights = 16	1	Weights = 8	1
0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	1	0	1	0	1
2	0	0	0	1	0	0	2	0	2
3	0	0	0	1	1	0	3	0	3
4	0	0	1	0	0	0	4	0	4
5	0	0	1	0	1	0	5	0	5
6	0	0	1	1	0	0	6	0	6
7	0	0	1	1	1	0	7	0	7
8	0	1	0	0	0	0	8	1	0
9	0	1	0	0	1	0	9	1	1
10	0	1	0	1	0	0	A	1	2
11	0	1	0	1	1	0	B	1	3
12	0	1	1	0	0	0	C	1	4
13	0	1	1	0	1	0	D	1	5
14	0	1	1	1	0	0	E	1	6
15	0	1	1	1	1	0	F	1	7
16	1	0	0	0	0	1	0	2	0

Table 1: Binary, octal, decimal and hexadecimal equivalents of the decimal numbers 0 through 16.

alphabet A through F are used to represent the numbers 10 through 15. To convert a binary number to hexadecimal start at the least significant end and count off binary digits in groups of four. If the last group does not contain four digits visualize additional 0s to make four binary digits. Consider each 4 digit group as a separate number and write its hexadecimal equivalent (refer to table 1). For example:

```
binary        11010111001000111
separated     0001 1010 1110 0100 0111
hexadecimal     1    A    E    4    7
```

To convert from hexadecimal to binary notation just reverse the procedure. Replace each hexadecimal digit with its binary equivalent, remembering to add leading 0s so that each of the hexadecimal digits forms a 4 digit binary number.

Octal conversion is the same except the binary number is broken into groups of three. For the previous example:

```
binary      11010111001000111
separated   011 010 111 001 000 111
octal         3   2   7   1   0   7
```

Conversion from octal back to binary is done by replacing each octal digit with its 3 digit binary equivalent.

Let's return to our 8 bit computer. If table 1 is expanded to eight binary digits (bits) the largest number that can be formed would be decimal 255 (binary 11111111). Counting 0, this gives 256 different numbers that can be expressed with eight bits. In some applications 256 numbers are enough, but if you were going to balance your checkbook a maximum balance of $2.55 would be rather useless. I will return to this limitation shortly and show you how to get around it; but first, in the context of balancing checkbooks, what happens when a number is negative? If we accept 0 as a positive number then we can assign one bit of the number to be the sign, a 1 for negative and a 0 for positive. Notice that we have lost a bit from the numerical value and now can only have 128 different values each with two signs for a total of 256 different numbers. However, –0 is not considered a valid number, so there are only 255 usable numbers. This type of notation is called a sign-magnitude representation of a number. Using this notation, –1 is written as:

```
       10000001
sign bit     magnitude
```

If you were going to add two signed numbers (say +3 and –1) your program

would have to take into account several things first. First, if you simply added the two numbers, the result would be wrong:

+3	00000011	
–1	10000001	
sum	10000100	= –4

Wouldn't it be nice if there were a number notation that would allow identification of positive and negative and give a correct answer when added together? Consider adding +1 to –1 to get 0. What 8 bit binary number added to 1 gives 0?

8 bit binary number	11111111
+1	00000001
sum	100000000

(overflow to ninth bit)

The binary number which is all 1s can be called –1. What would –2 be?

–2	11111110
+2	00000010
sum	100000000

We can take any positive number up to 127 decimal (01111111 binary) and subtract it from 0 (assume there was a ninth bit equal to 1 so 0 is really 100000000). The resultant binary number is called the 2's complement. The most significant (leftmost) bit is a true sign bit in the 2's complement notation, but negative numbers have an altered magnitude value. When two such 2's complement notation numbers are added the answer is correct. Consider the previous example of adding +3 and –1:

+3	00000011
–1	11111111
sum	100000010 = +2 (in 2's complement notation)

Now consider adding +1 and –3:

+1	00000001
–3	11111101
sum	11111110 = –2 (in 2's complement notation)

One method of finding the 2's complement of a number has been mentioned which required subtraction from binary 0. A simple method that can easily be done on paper, especially if you are prone to making errors in binary subtraction like me, is to first rewrite the number substituting 1s for 0s and 0s for 1s, then add binary 1 to the result. For example, the 2's complement of +5 is:

+5	00000101
substitute	11111010
add 1	1
–5	11111011

To check, we should be able to take the 2's complement of –5 and end up with +5:

–5	11111011
substitute	00000100
add 1	1
+5	00000101

Substituting 1s for 0s and 0s for 1s is called complementing and is usually found as an instruction in the computer instruction set. Adding 1 is usually available as an instruction also. Sometimes both instructions can be combined into one step. In summary, to make a number negative (if you have no negate instruction):

- Clear the accumulator.
- Add the number to the accumulator.
- Complement the accumulator.
- Add 1 to the accumulator.

The accumulator now contains the negative of the original number in 2's complement notation. One interesting property which comes along with this 2's complement form is the fact that *all* states of the 8 (or n) bits are valid and there is only one zero state. The largest negative number, however, has no positive value equivalent.

Let's return to the problem of not having enough bits to make a big enough number. If we use two successive byte size memory locations to represent a number we have 2^{16} (65,536) possible numbers. Using 2's complement notation we can have any number from –32,768 to +32,767. If that is not enough you can expand in increments of eight bits until your needs are satisfied. There is a problem now, since the computer only operates on eight bits at a time. When a number is spread over more than one memory location it is called a multiple precision or extended precision number. If two locations are used for each number it is

called double precision; if three are used it is called triple precision, etc. (However, it remains a binary number. In large machine floating point representations this terminology has a different meaning.)

One more item needs to be mentioned before I describe multiple precision arithmetic. All computers have some sort of means to detect an accumulator overflow (or underflow). In our 8 bit example this is a ninth bit at the extreme left of the number. The status of this bit can be controlled and tested. It increases by 1 when the addition of the eight bits causes a carry and decreases by 1 when the subtraction of the eight bits causes a borrow. When a rotate instruction is executed this bit receives the most significant bit and loads the least significant bit on a rotate left. It receives the least significant bit and loads the most significant bit on a rotate right. This extra bit is known by different names, such as overflow, carry, and (in the PDP-8) the link.

The steps shown in the box will vary from machine to machine, depending upon how the instruction set is organized. For example, the 6800 instruction set has ADC for add with carry input, and the 8080 instruction set has a similar variation. In these cases, there is no need to rotate the accumulator from the carry flag prior to the second addition, since the ADC instruction type takes into account the old value of the carry.

How do you do a 2's complement of a double precision number? Start with the accumulator and carry set to 0s. Add the least significant part of the number. Complement and add 1 as before. The accumulator now contains the 2's complement of the least significant part, so store it. Rotate left to load any carry into the least significant bit. Store the contents of the accumulator (the carry) in any convenient location. Add the most significant part of the number to the accumulator. Complement it only. Now add the previously stored carry. The contents of the accumulator are now the most significant part of the 2's complement. As in the simple addition case, machines with an ADC instruction can often use the previous setting of the carry flag as part of the addition.

Addition

All computers can add. They typically add some specified memory location to the contents of an accumulator (a built-in memory location in the processor). When adding two or more numbers together you must be careful not to allow the resulting sum to get so large that you get an incorrect answer. For instance, when using 2's complement notation you can add together two numbers which are positive and get a negative answer if a carry into the sign bit occurs. Also be sure the accumulator and carry are initialized to 0.

Subtraction

Some computers do subtraction directly, but be careful. They may only subtract magnitudes. You have to do

An Example of Double Precision Addition

Step Number	Procedure	Resulting Values: Carry Bit	Resulting Values: Accumulator
1&2	Clear carry bit and accumulator.	0	0 0 0 0 0 0 0 0
3	Add A_2 to the accumulator.	0	1 1 1 0 1 0 0 0
4	Add B_2 to the accumulator (gives C_2 in accumulator).	1	1 1 0 0 0 1 0 0
5	Store contents of accumulator in the memory location assigned for C_2. Set accumulator to 0; preserve status of carry bit.	1	0 0 0 0 0 0 0 0
6	Rotate accumulator left one bit.	0	0 0 0 0 0 0 0 1
7	Add A_1 to the accumulator.	0	1 1 0 0 1 1 1 0
8	Add B_1 to the accumulator (gives C_1 in accumulator).	0	1 1 1 0 0 1 1 1
9	Store contents of accumulator in the memory location assigned for C_1. Set accumulator to 0.	0	0 0 0 0 0 0 0 0

To check, write out all 16 bits and add:

```
A =  1 1 0 0 1 1 0 1 1 1 1 0 1 0 0 0
B = +0 0 0 1 1 0 0 1 1 1 0 1 1 1 0 0
C =  1 1 1 0 0 1 1 1 1 1 0 0 0 1 0 0
```

$$A \begin{cases} A_1 = 1\ 1\ 0\ 0\ 1\ 1\ 0\ 1 \\ A_2 = 1\ 1\ 1\ 0\ 1\ 0\ 0\ 0 \end{cases} \qquad B \begin{cases} B_1 = 0\ 0\ 0\ 1\ 1\ 0\ 0\ 1 \\ B_2 = 1\ 1\ 0\ 1\ 1\ 1\ 0\ 0 \end{cases}$$

The simple addition of two double precision positive numbers, A and B, to obtain an answer C. In this example the subscript 1 denotes the most significant part of the number and the subscript 2 denotes the least significant part. To add two double precision numbers:

1. Clear the accumulator to all 0s.
2. Set the overflow, carry (or whatever the extreme leftmost bit is called) to 0. Often these two steps can be combined into one.
3. Add A_2, the least significant part of A, to the accumulator.
4. Add B_2 to the accumulator. At this point the accumulator contains the sum of the least significant parts of A and B. If any carry has occurred due to this addition the carry bit will be a 1. If no carry has occurred, it will be 0.
5. Store the contents of the accumulator in the memory location assigned for C_2. Set the accumulator to 0, but preserve the state of the carry bit.
6. Rotate the accumulator left one position. This will load the carry bit from the previous addition into the least significant bit of the accumulator.
7. Add A_1 to the accumulator.
8. Add B_1 to the accumulator. At this point the accumulator contains the sum of the most significant parts of A and B plus any carry from the least significant parts.
9. Store the contents of the accumulator in the memory location assigned for C_1.

checking of each number to see which is larger and in what order the subtraction takes place in order to determine ahead of time what the sign should be. Sign bits must be set to 0 so they don't give false indication of magnitude. The sign bits must be put back into the answer if you are using signed number notation. All of this takes a lot of extra software and time. If you are using 2's complement notation you can subtract directly and the sign will automatically come out correct. Most of the common microprocessors use 2's complement notation and have no problems subtracting directly.

If direct subtraction is not possible in your computer, all is not lost. Consider subtraction by addition of a negative number. If you want to perform A–B=C, for example, use 2's complement notation and first make B negative by taking its 2's complement and then add A to get the answer C. Notice that even if A or B is negative to begin with, the answer will still be correct in 2's complement notation without any extra software to keep track of the sign. This will also work for multiple precision numbers. You still have to be careful not to use numbers which are large enough to cause inadvertent sign bit changes.

Multiplication

Two problems immediately confront us when we consider multiplication. First, if you multiply two 8 bit numbers together, the result is 16 bits long; and second, you simply can't add up 2's complement numbers and always get the correct answer. For instance, if you add –3 three times the answer would be –9 (equivalent to 3 times –3) which is correct, but what would you do with a negative multiplicand as in –3 times –3? To solve this problem and use successive addition to do multiplication the first step is to convert all numbers to a positive absolute value without sign. If you have been using 2's complement notation it is an easy procedure to convert. Rotate left to load the sign bit into the carry bit. Test the carry bit. If it is 0, the number is positive; if it is 1, the number is negative. If the number is positive, just rotate right to restore it to its original value and set all 0s into a location assigned to be the sign of the number. If the number is negative, first rotate right to restore the original, then take the 2's complement of it to get the number positive and finally, with an all zero accumulator, set the carry bit to 1 and rotate right. Store this in the sign location. What we have done is separate the number into its sign and magnitude. Now if the signs are added we get the correct sign for the answer directly which should be stored in a location assigned to the sign of the answer. Two generalized techniques may be used to find the magnitude of the answer.

Successive addition may be used by adding A to itself B times. If the instruction set allows decrementing a number, use that instruction to decrease B by 1 each time you add A to the accumulator until B reaches 0. At that point you have the magnitude of the answer. If the instruction set allows incrementing but not decrementing, first take the 2's complement of B and use incrementing of the now negative number until it reaches 0. The disadvantage of using successive addition is that you have to do a potentially large number of additions which can take a lot of time.

A second technique that requires only a few operations is a direct copy of how you do binary multiplication by hand. For example, let's multiply two 4 bit binary numbers by hand:

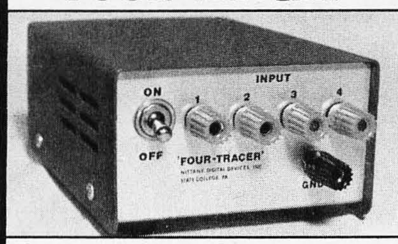
```
      1101     = A
    X 1010     = B
      ----
      0000
     1101
    0000
   1101
  --------
  10000010     = C
```

Notice that all we have to do is add A, a shifted version of A or 0, depending on which digit of B is used and whether it is a 1 or 0. Notice also that two 4 bit numbers produce an 8 bit answer, so if you don't restrict the number size, you have to use multiple precision shifting and addition.

A technique that is sometimes useful when you want to multiply by a constant is to recognize that shifting a number left one position is equivalent to multiplying by 2. Shifting left two positions is equivalent to multiplying by 4, three positions is multiplying by 8, etc. By shifting and adding the various shifted numbers in a fixed format you can do the equivalent of multiplying very quickly by a constant. For example, to multiply by 5, shift left twice and add it to the original:

$$5A = (4 + 1) A = 4A + A$$

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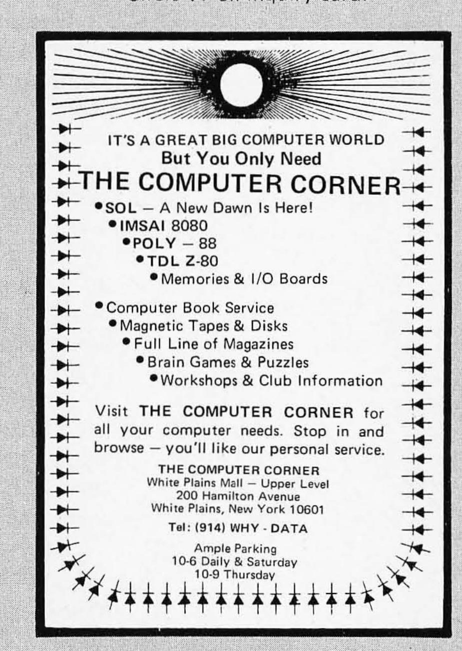
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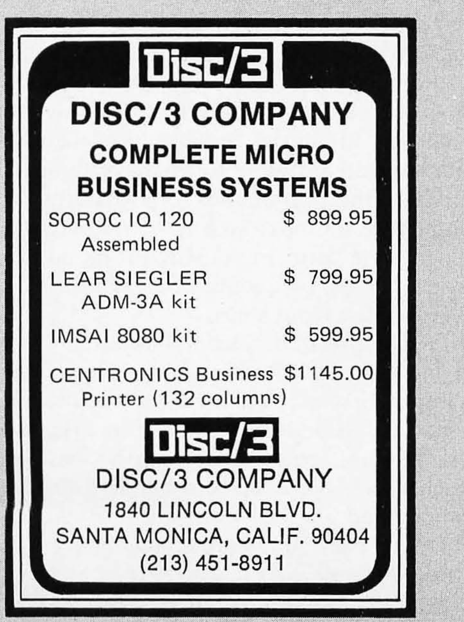


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Division

Division is the most difficult operation to do. First, handle the separation of magnitude and sign as under multiplication and use the same technique of adding signs to get the correct answer sign. The problem with division is that seldom does the answer come out exactly even. Usually there is a remainder. You have to decide how far you want to carry out the answer and what rules you are going to use for rounding off. You may also have the binary equivalent of a decimal point to consider.

One method of dividing is by successive subtractions. For example, to divide A by B, count how many times you can subtract B from A before the remainder is 0 or negative. If the remainder goes to 0, the value of the count is the exact answer. If the remainder becomes negative that means you went one step too far. Reduce the count by 1, add B back to A, and test the remainder to see how to round off. This will give you a whole number answer. It will also locate the binary equivalent of a decimal point if you want to carry the answer further.

Alternatively, you can add B successively, counting the number of times, until the sum equals or exceeds A. Equal to A means the answer is exact, and exceeds A means you went one step too far.

One very limited type of division is very easily done. If you are dividing by 2,4,8,16, etc, all you have to do is rotate the number to the right the appropriate number of times. However, you must be careful of rotating a 1 through the carry bit and having it appear in the most significant bit of the number. To avoid this be sure the carry bit is cleared to 0 before each rotate. A check of the carry bit after the last rotate can be used for round off determination. If it is a 1, round off the answer to the next higher number.

Interfacing to a Nonbinary World

As mentioned earlier, the world is decimal oriented and we should be able to talk to the computer with decimal digits, and indeed our terminals have decimal keys and decimal outputs. Our terminals, however, talk to our computers in yet another language, usually ASCII.

Notice the codes for the decimal ASCII digits 0 through 9 as seen in any table of ASCII codes. If you consider only the least significant four bits you have the binary value of the associated decimal digit. There are two ways of extracting the binary value from the ASCII code. You can first load the ASCII character into the accumulator and then subtract 0110000 or mask it by "anding" the accumulator with 1111. So now you have converted one decimal digit into its binary equivalent. Unfortunately, very often you need more than one decimal digit to make the number. The simplest way to handle this is to use a fixed format. This means you have to enter leading 0s so a number will always have the same number of digits and the order in which they are entered defines their decimal rank (units, tens, hundreds, etc). Since each digit is now known it may be placed in a location assigned to its rank after it has been converted to binary. You now have a fragmented number which is not usable for arithmetic. It must first be made into a single binary number.

As an example, let's assume we are using a 3 digit fixed format and the decimal number we are entering is 27. First we type a 0 for the hundreds digit which is stored in a location, HUNS, as a binary 0, using one of the ASCII to binary conversion techniques. Then we type a 2 and a 7 which are converted to binary and stored in locations TENS and UNITS, respectively. Now to make it all one big binary number.

First test the hundreds digit. It is 0 in this case, so jump to testing the tens digit. It is not 0, so multiply the binary equivalent of 10 (1010) by the contents of the TENS location, in this case 2, and the contents of the UNITS location, and store it in the answer location. In the more general case what you do is multiply each decimal digit by the binary equivalent of its rank and add up all the partial products. Finally, you have to convert the binary number into whatever notation you are using for doing arithmetic.

After the arithmetic, or whatever, is completed, the next step is to output it in recognizable form (ie: ASCII to the output device). The procedure is essentially a reverse of the input steps.

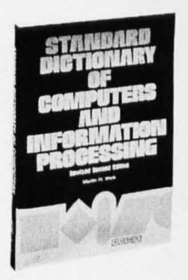
First convert the binary number into its fragmented equivalent. Using the above example, first subtract the binary equivalent of decimal 100 (1100100). In this case, the first attempt produces a negative answer, which means there are zero hundreds in the number and the HUNS location should be set to 0. Next try subtracting binary 10s until the result goes negative, then add one

back. The number of times you can subtract 10s before it goes negative is equal to the value of the 10's digit. The remainder is the value of the units digit. These digits may now be converted to ASCII by simply adding 0110000 to each digit location. The final step is to transfer each digit (now in ASCII) to the output device (TTY or CRT terminal, etc) in the proper order.

It is possible to write a program that will work under a variable format for input and output to eliminate the need for leading 0s. This is more complicated since you have to count how many individual entries of digits are made and then arrange them in reverse order knowing the last entry is the units digit regardless of how many digits there are.

One last point: always verify each arithmetic program you write, either in the computer (best way) or write it out step by step by hand. Use extreme values for numbers like 0, 1, and the [redacted]

Book Reviews



Standard Dictionary of Computers and Information Processing, revised 2nd edition *by Martin H Weik, Hayden Book Company Inc, Rochelle Park NJ, 1977, 400 pp, 6 by 9 inch, hardbound, $16.95.*

Reviewing a dictionary is usually a simple straightforward task. How much can one really say about a book of definitions? Aside from stating whether or not the dictionary gets the job done, how else does one discuss its attributes? Normally, I would agree to let the matter drop with a few quick sentences. This time, however, I don't feel that that kind of treatment is really adequate.

In Weik's dictionary we have the most comprehensive collection of computer software *and* hardware terms I have seen to date in one volume. While not as detailed as some books have tried to be, Weik's book still manages to give clear, concise explanations of the items included. This is accomplished by liberal use of cross-indexing and by the supportive use of excellent illustrations and examples. Particularly impressive are the electronic diagrams which even a novice could understand.

In addition to the over 10,000 terms included from the first edition of the dictionary, some 2500 terms from areas such as microprocessors, minicomputers, computer networks, modems, coding schemes, data base theory, and information theory have been added. All of the original definitions have been reviewed to ensure that they are up to date as well.

This book is not without its flaws. The indexing is quite often confusing, eg: for "bus driver" one is told to look under "driver, bus." But at least the user is directed by the text, which is more than can be said for a lot of dictionaries which never give a clue as to where to look for the definitions of a phrase. There are some dubious inclusions, such as the definition of "machine," as well as many omissions, particularly in the area of microcomputer hardware.

However, this book is good for quick, simple, accurate definitions of a lot of useful terms. No reference shelf would be complete without it.

Blaise Liffick, Editor■

Mounting a Paper Tape Reader

Jack Bryant
Mathematics Department
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College Station TX 77843

Several months ago I ordered a RAECO paper tape reader. It arrived (a near record) 12 days later. Its very complete documentation, seven mimeographed pages, included a mounting template and circuit diagram. For $32.50 postpaid, it has to be a "best buy" among paper tape readers. But where could I mount it? Some unused panel space on my SwTPC 6800 processor's box seemed ideal.

The RAECO documentation suggests a 100 W light bulb 1 foot above the reader for illumination. This seemed a little extreme, and while looking around the junk box for something less blinding, I ran across a metal snuff box and a brass cable clamp. I could vaguely recall having seen some automobile lights with a linear filament. Sure enough, the Eveready #211 (two bulbs for $.79 at an auto parts outlet) fit exactly. Photo 1 should tell most of the story.

I removed the front panel from the computer (this is for a SwTPC 6800 system) and used the template furnished by RAECO and a sabre saw to cut a hole for the reader. I soldered the brass clamp to the lid of the snuff box and drilled three holes through the lid and panel. I then used 1/8 inch aluminum pop rivets in two of the holes to fasten the lid to the panel. My cable clamp was tight enough to mount the light bulb so I didn't have to use any other fasteners. I soldered a wire to the light bulb end sticking out and ran it through the one remaining hole. (The tip of the bulb base is the only place which will take ordinary solder.) Figure 1 shows two possible alternatives for a lamp power source; I used alternative a. Chassis ground furnishes the return. Since the light bulb is being run on (at most) 4 V, it should last forever.

For the cover, I drilled a few 1/4 inch holes in the snuff box top with a broom handle used to back up the top during drilling. (Mind your fingers, it tends to slip away easily.) I used a file to smooth out the rough spots, and then finished everything off with a coat of black paint.

The RAECO optical paper tape reader Model TPR-1 is available from RAECO, POB 14, Readville MA 02137.■

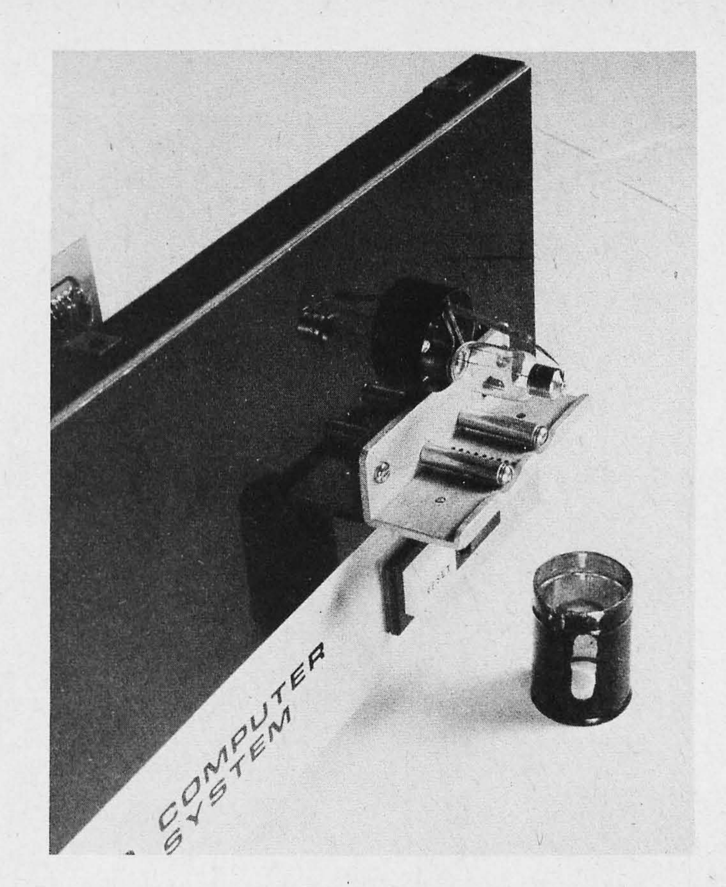
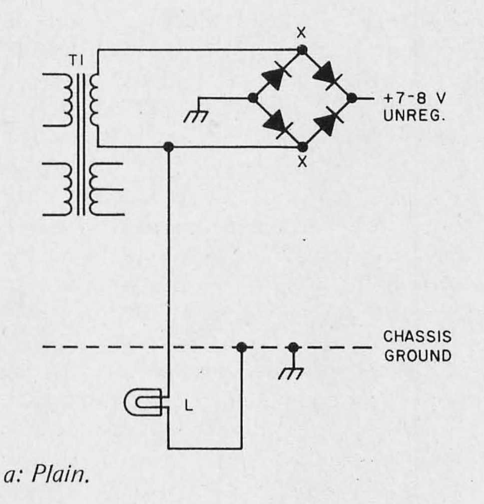
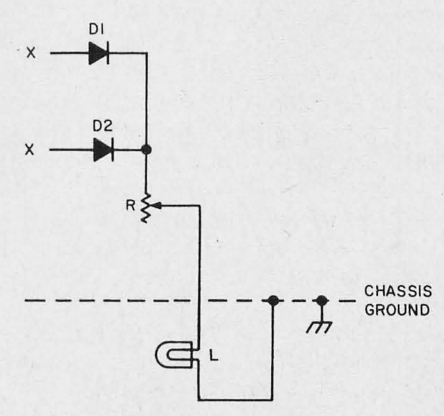


Photo 1: The RAECO tape reader, installed in an SwTPC 6800 system with an automobile lamp and homebrew enclosure above the sensors.



a: Plain.



b: Fancy; D1 and D2 can be 1N4001, R 20 ohms, 10 W.

Figure 1: Lamp (L) is an Eveready #211 12 V automobile dome lamp. T1 is the SwTPC 6800 power transformer. I used the 7.25 V winding.

Notes on Bringing up a Microcomputer

Sol Libes
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About the Author

Sol Libes is an enthusiastic microcomputer user, president of the Amateur Computer Group of New Jersey, a teacher at Union County Technical Institute in New Jersey, and author of several books on digital logic and microcomputers.

The following is my recommended procedure to follow when building a microcomputer from a chip set. This procedure makes the assumption that you've already acquired or drawn up a complete set of plans from which to wire your computer. Many people follow this route, as opposed to the kit route, particularly since manufacturers, such as Intel, have sold chip sets to schools and students at special reduced prices. Designing then building a computer is a great way to learn about the hardware required in microprocessor systems. However, these tips can also be used in troubleshooting kits. Getting a homebrew computer up and running and debugged requires this sort of step by step technique, so that elimination of errors is made as easy as possible through checkout as each new element is introduced.

Start by wiring up the microprocessor chip itself. Connect the power supply lines to the integrated circuit socket. Without the microprocessor chip in the socket, turn on power, check the voltages at the proper terminals of the socket and verify that they are correct. This is important since microprocessors (and other integrated circuits) are not very tolerant of incorrect supply voltages.

Next, connect up the clock circuit and install the microprocessor itself. Turn on power and check the clock signal at the pins of the microprocessor socket with an oscilloscope. The scope should be a DC coupled unit with good frequency response; 20 MHz or better is desirable but in a pinch a 10 MHz scope can be used. Check that the correct phase relationships exist between the clock pulses. For example, with the 8080 microprocessor the pulse widths and spacing are quite critical, and must be within the specifications on the manufacturer's data sheet or strange things can happen. Be sure the clock frequency is correct. An oscilloscope can typically measure this to about 5% accuracy, with higher accuracy possible if you calibrate against a reference frequency or use a good frequency meter instead. In systems utilizing programmable timers, incorrect clock frequency can cause interface problems.

If everything checks out so far, then it is time to let the microprocessor chip execute an instruction. Still without any memory connected, the microprocessor can execute an instruction.

For example, on the 8080, we can tie the data lines low causing the execution of a NOP (00) instruction. An even better procedure is to let the data and memory address lines float (nothing connected). This will cause the RST7 (FF) instruction to be found on the data lines. This restart instruction will execute a call to a subroutine, an operation which pushes information onto the stack (which does not exist at this time). Since no memory is present, and the instruction does not change, an "infinite loop" of RST7 instructions results. The net result is that the address lines of the processor will scan

through all the addresses in memory as return addresses are continually pushed onto the stack. The 8080 processor will continue cycling through all the memory address locations, even though no memory is connected. Similar test conditions can be established with other microprocessors as well.

Now, with the memory still disconnected, connect an oscilloscope to each address line and check that it is cycling through the 64 K addresses of a 16 bit address space. You should see a count in binary fashion as shown in figure 1.

If any of the adjacent memory lines are shorted together, a very common problem, you will see the lines changing together. In this case, check carefully for solder bridges (if your processor was built from a kit) or shorts (if hand wired) between adjacent memory address lines. If there is no signal on any line, check for disconnections. Be sure that the addressing is sequencing in the correct binary order before proceeding further, for the processor must produce a valid address sequence under dummy instruction conditions if it is to do useful processing later.

If you use the NOP (no operation) instruction the same pattern should be observed; the use of a NOP instruction is required in most processors for this test.

In many processor designs, a set of buffer integrated circuits is used to isolate the external address and data buses from the processor in order to provide a higher power drive capability. If your processor design employs such buffering circuits, the next step is to wire up the sockets for these buffers and associated control logic. Then you should install the buffering integrated circuits after checking all power wiring. Then the tests performed for the processor alone can be repeated, looking this time at the outputs of the address buffers, and using the data bus buffers' system side to present the RST7 (8080) or NOP instruction to the processor side of the data bus buffers.

If everything is correct to this point, then connect up the memory. Wiring up a memory board is done in a manner quite similar to that used in getting the processor itself going. The first step is to complete all wiring and check out power voltages at the memory integrated circuit sockets. Then plug the board into the system and repeat the processor address test described previously to verify that the address lines at the typical memory socket and at inputs to decoding logic are functional. The low order lines of a memory address typically go directly to memory integrated circuits.

After the directly connected address lines are verified in the system, turn off power and plug in the integrated circuits for address decoding of the high order address lines to the memory board. With the system powered up again, repeating the NOP loop test should show decoding of the memory board select for some percentage of the time it takes to cycle through all addresses, and decoding of various chip selects for a smaller percentage of time. Thus if the memory board is an 8 K byte board with 4 K bit static chips, board select should be decoded 1/8 of the time (12.5 percent duty cycle) and chip select for each 4 K byte segment should be decoded 1/16 of the time (6.25 percent duty cycle) as the processor cycles through all possible addresses.

Once decoding of the memory board has been verified, remove power again, and install all the memory integrated circuits of

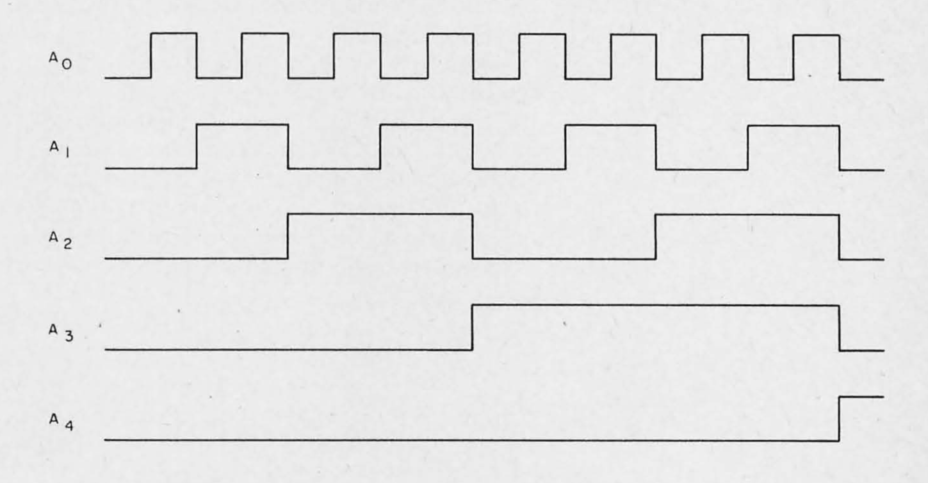


Figure 1: Much of the behavior of a system can be checked out simply by looking at the address bus: the lines which contain the processor's current requests to memory address space. The simplest initial test of a processor is some form of null operation loop which continuously scans all possible addresses in memory address space. When observed with an oscilloscope, such a loop (see text) will produce a regular set of square waves with the lowest frequency on the high order address bit and the highest frequency on the low order address bit. Here we see the expected scope display as the probe is applied (top to bottom) to address bits A_0 thru A_4.

the system as well as memory board output bus drivers.

At this point, we make the assumption that your processor design includes some method of setting the contents of memory. This might be a set of toggle switches which can take over the address and data bus from the processor in order to load memory. It might also be use of a read only memory monitor program which you write, thoroughly desk debug, and program into read only memory circuits. Whatever the method is, the details necessary for loading memory manually must be wired up and tested next. Now try entering a very short program which will put the processor in a tight loop. The shortest and simplest loop possible is a single jump instruction, repeatedly jumping to itself. For example, on the 8080, if the program should be located at hexadecimal memory address 0000 it would be as follows:

```
0000  C3 00 00   JMP 00 00
```

When this program is executing, check the memory address lines and data lines with the scope. You will observe the memory address lines counting only the three addresses and at the first address time hexadecimal C3 should be observed on the data bus lines. At all other times the data bus should be hexadecimal 00.

If things look good so far, then wire up an output port (00 is a good one for an 8080). As with the other segments of the design, the wiring of the output port sockets comes first, then power pins are tested thoroughly. Finally, the appropriate integrated circuits are inserted into the sockets of the IO port logic and we can proceed to check it out. In this example, a simple latched 8 bit output port is used for purposes of illustration. Write a minimum program to check its operation. The following little program can be used on the 8080:

```
0000  D3 00         OUT 00
0002  C3 00 00      JMP 00 00
```

This very tight loop will cause a pulse to be generated on the "out" control line. Check for the presence of this pulse. Check the memory address lines for the correct counting pattern and the data lines for the proper data patterns. This should be done with the scope synchronized by the out pulse which occurs once each time around the loop. With the scope synchronized in this manner, it is possible to check the memory address lines and data lines to be sure that the correct logic levels are occurring at the proper times in the execution loop.

If operation is not correct check the data lines for shorts or opens. Shorts usually occur between adjacent lines which means that identical bit patterns will be observed on adjacent lines. Opens lead to missing bit patterns on the open lines.

Now check the operation of the output port with the following 8080 program loop:

```
0000  3C            INR A
0001  D3 00         OUT 00
0003  C3 00 00      JMP 00 00
```

This will cause a binary count bit pattern to appear on the data lines of 8080 output port 00. These lines should be checked with the scope. Again check for shorts between adjacent lines and opens.

If operation of longer programs is not correct, but the previous short loops operated correctly, then check for swapped high order memory address lines. This will usually cause unexpected jumps in the execution of the program. Or if the processor seems to be executing every other instruction, check for an open address line.

A final thing that you should do after you get the system running is to look at the response times on the bus. Check to see that the data coming back to the memory is within the proper timing relationships as found in the manufacturer's specifications. Check to be sure that the data is stable before the microprocessor strobe occurs. Problems may be caused by slow memory chips and can lead to unexpected random errors in execution of a program. Such specifications should be checked under "worse case" conditions (such as at elevated temperatures) so that when normally running the system timing errors do not occur with any significant probability.

These steps are typical of the methodical process of checking out (and building) a new computer system. The considerations discussed here are typical, but by no means cover all the possible systems and all possible conditions to check out. Once you get to the point of executing programs, most of the crucial steps have been successfully accomplished.

A key point to remember is that digital hardware only does what you tell it to do by way of design and wiring. Finding bugs in new hardware, like finding bugs in programs, is a process of setting up key conditions of the system then checking actual responses against those to be expected if the system were working perfectly. It requires a willingness to learn to understand the expected modes of operation, plus a bit of ingenuity.■

Technical Forum

A Note on Advances in Technology

Paul Robinson
932 Olive Av
Coronado CA 92118

A Note on Advances in Technology

Since it seems that megaword computers are of high interest, readers might be interested an article in the May *Scientific American,* page 36, about "Amorphous Semiconductors" for memory applications. This development offers higher density, lower complexity, lower costs (because of manufacturing method) and higher reliability than any of the recently marketed magnetic bubble memory systems, plus the cycle times are far below anything in common use, 50 to 100 ns and even lower times anticipated in the near future. After reading about "Amorphous Semiconductors" it is very apparent that they are going to play a major roll in changing the world of computing on a scale matched only by that of the innovation of LSI chips a few years ago. I'll be watching BYTE for further developments in this line.

See also a recent Scientific American *article on the physics of synchrotron radiation, and the possible effect of small X-ray synchrotron technology on the fabrication of ordinary crystalline integrated circuits with X-ray lithography. The article "Uses of Synchrotron Radiation" was in June 1977* Scientific American, *written by Ednor M Rowe and John H Weaver. The reference to X-ray lithography is found on page 41 and begins "Further afield, synchrotron radiation promises to transform the technology employed in making integrated circuits. . ."*■

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The Motorola 6809: Some Rumors from Austin

Notes by Carl Helmers

For some time now, it has been general knowledge that Motorola is working on a new design for a microprocessor to be made available at some unspecified time in 1978. Recently, I elicited some advance information that suggests some of the major features of the new Motorola 6809 design: information well worth sharing with readers.

The new Motorola 6809 is going to be an evolutionary design improvement creating a major new processor architecture that will be a joy for both low level programmers and designers of systems programming. One of the major enhancements is the increased ability to do 16 bit arithmetic and indexed addressing relative to the older 6800 design. A rundown of the new architecture reveals the following features:

- The A and B registers of the 6809 act like the separate accumulators of the 6800, but can also be concatenated A:B to become the 16 bit "D" accumulator (double accumulator). This D accumulator can be used for the usual 16 bit arithmetic operations of addition, subtraction, load, store, and comparison.
- Expansion of the indexing capabilities with the inclusion of a second "Y" index register 16 bits wide, thus allowing the processor to maintain two 16 bit index registers. As anyone using the 6800 can attest, a major portion of the code often boils down to loads and stores of the index register in order to use memory to emulate existence of two index registers. This technique will not be needed with the 6809.
- Addition of one more 16 bit stack pointer, the "user stack," which can be used together with the existing systems stack to enhance data management techniques.
- And of course, with a wealth of 16 bit pointers in the processor, the 6809 design implements all the register to register transfer operations and register to memory (memory to register) transfers one might expect, including stack operations.
- With all this machine state data sitting around in the processor, what happens when an interrupt occurs? People have occasionally complained about the time taken by the complete state save done by the 6800 in response to an interrupt; the wealth of data on the 6809 compounds this timing problem. Motorola's answer with the 6809 is to create a new additional hardware interrupt input line, the "fast interrupt" line, which accomplishes the vectoring of the interrupt while saving only the return address and the condition codes. (When such fast interrupts are used, it is of course the programmer's responsibility to take care of preservation of any registers or machine state information used in the interrupt handling routine.)

Care and Attention to Addressing

With all the 16 bit pointers present in the 6809 design, one might ask: "Why?" The basic reason for incorporating such pointers in the design is to achieve a number of benefits in the process of calculating addresses. Since in any large system, a good portion of the tricky problems of software design concern allocating and managing memory address space resources, this makes the 6809 a very attractive high level language machine. Features concerned with address calculation include:

- Extension of program counter relative references beyond the concept of relative branches (and long relative branches) to include data references using the program counter as an index or base register.
- Addition of a fast multiplication (8 bit operands, 16 bit unsigned product) operation to enhance calculation of array offsets in high level language code.
- Existence of the user stack concept for data management independent of program flow management at run time.
- A full complement of indexed addressing modes, with 0, 5, 8, or 16 bit offsets, allowing indirecting, "auto increment" or "auto decrement" indexed references with increments of 1 or 2, from either index register *or* either stack pointer.

Miscellaneous Hardware Features

All this attention to the software orientation of the 6809 architecture by the engineers at Motorola is not without equivalent attention to the hardware details. Useful new hardware features include an on chip clock design which requires simply an external crystal to set frequency, a slow memory wait line which allows for long memory access cycles (or contention in multiprocessor systems), and the introduction of an instruction fetch synchronization signal that can be used to advantage by hardware hackers who want to know when instruction is begun for reasons as varied as the number of systems applications for such a machine.

Anticipations. . .

This information on the Motorola 6809 is a substantial rumor about current information on the design; further details must await final design, which is currently in progress. But from what I've heard to date, it looks like the 6809 is well on its way to becoming a software oriented "dream machine" among microprocessors. Readers can expect more definitive information on this processor toward the middle or end of 1978 when Motorola releases more official information. Perhaps we'll see some personal computer products with the 6809 as their central processors toward the first part of 1979. Designers of new products in that time frame would be well advised to take a look at whatever preliminary information Motorola can be cajoled to release about this new product. ■



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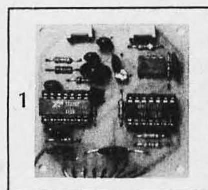
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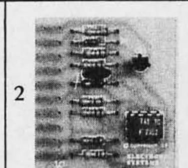
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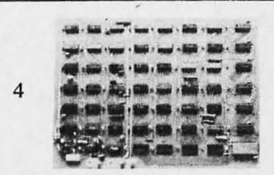
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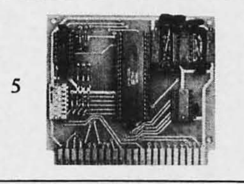
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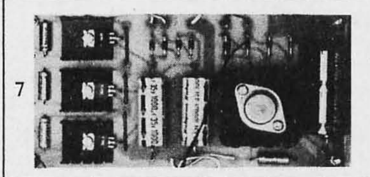
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(408) 374-5984

Circle 41 on inquiry card.

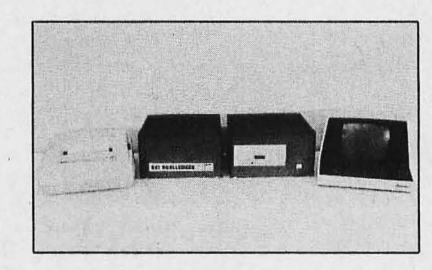
A Personal Computer from Olivetti



The Olivetti P6060 Personal Minicomputer features built-in extended BASIC, a printer with plotting capability and a wide variety of interfacing options for peripherals. The system includes up to 80 K bytes of programmable memory accommodating both the operating system and a user working file (8 K to 48 K bytes), single or dual drive floppy disk, 32 character upper and lower case ASCII display, 80 column, 80 character per second thermal printer, and a keyboard with special function keys and 1 key abbreviations for most BASIC keywords. The printer features graphics supported by system software for scaling, framing, offsetting, axis drawing and alphanumeric labeling. The extended BASIC features random file handling and matrix operations. Two standard character serial IO ports, an RS232 interface, and a direct memory access (DMA) channel are available for interfacing the P6060 to a wide variety of devices. A basic configuration with 8 K user memory and a single floppy disk is priced at $7950, while a system with 16 K user memory and dual drive floppy costs $10,000. For more information contact Olivetti Corporaton of America, Personal Minicomputers, 500 Park Av, New York NY 10022, (212) 371-5500. ▪

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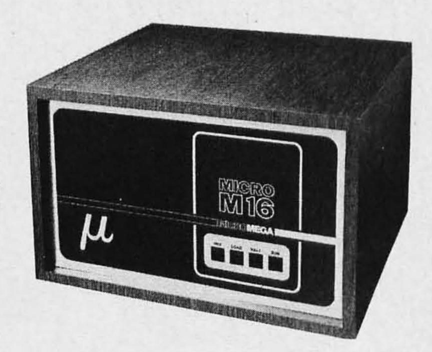
Complete Disk Based System for $2599



The complete OSI Challenger system includes a 6502 processor, 16 K of programmable memory, a system monitor and disk bootstrap in ROM, a floppy disk based on the GSI 110 drive, and a stand alone CRT terminal with a Sanyo video monitor. Software includes a disk operating system, a disk based assembler and editor, a debugger with breakpoint, high speed dump and disassembly capabilities, and an 8 K disk based BASIC with multidimensional arrays, strings, a full complement of mathematical functions, and machine language access features. The complete system is priced at $2,599, or $2,099 without the CRT terminal and monitor. Options include a dual drive floppy disk for $1,590, and 13 accessory boards which provide up to 192 K bytes of programmable memory, 16 K bytes of EROM, digital to analog and analog to digital conversion, parallel and serial IO, cassette interface, video graphics display, and multiprocessing capabilities. Also offered are two dot matrix printers by OKI Data, the CP110 which prints 80 character lines at 65 lines per minute for $1,500, and the Model 22 which prints 132 character lines at 125 lines per minute with upper and lower case and form size control for $2,900. The Challenger is available from Ohio Scientific Instruments, 11681 Hayden St, Hiram OH 44234, (216) 569-7905. ▪

Circle 572 on inquiry card.

16 Bit Computer Features National PACE



This fully assembled unit offers an expandable system built around the National PACE 16 bit microprocessor. The Micro M16 comes with an EROM bootloader, low and high speed current loop and RS232 serial ports, and two 1200 bps audio cassette ports. A mother board accommodates up to four memory cards, each with 16 K 16 bit words of programmable memory, four IO cards, and an optional front panel card. A parallel IO port card includes two 16 bit input and two output ports as well as EROM sockets for IO device handler software. System software includes an 8 K macroassembler, a linking and relocating loader, a conversational editor and a debugger with spanshot and breakpoint capabilities. The M16 provides 8 K PACE BASIC which features direct IO and memory access, waits for input or timer, built-in hexadecimal conversion and program tracing for debugging purposes, as well as the usual BASIC language features. Enclosed in a gunstock walnut veneer cabinet, the M16 is available from Micromega Corporation, 11311 Stemmons Fwy, Suite 12, Dallas TX 75229, (214) 231-4777. ▪

Circle 573 on inquiry card.

Intelligent Terminal with Floppy Disk



The Omron 8035 combines an 8080 based programmable intelligent terminal with a floppy disk subsystem to create a complete program development facility. The system includes 20 K to 65 K bytes of programmable memory, 500,000 bytes of space on a dual drive floppy disk, an RS232 interface operable at rates up to 9600 bps, and an FDOS operating system with editor, assembler and debugger. Priced from $7,200 in single quantities depending on the configuration, the 8035 is available from Omron Electronics Inc, 432 Toyama Dr, Sunnyvale CA 94086, (408) 734-8400. ▪

Circle 571 on inquiry card.

OSI's Model 500 Computer

Ohio Scientific has announced the new Model 500 processor board can be used as a stand alone computer or as the processor in a larger system. The board accepts 8 K or read only memory, 4 K of programmable memory, 750 bytes of programmable read only memory, an ACIA-based serial port, a 6502 processor, and full buffering for expansion. It is available completely assembled with an 8 K BASIC package for $298.

The Model 500 is software and hardware compatible with Ohio Scientific's 400 kits and Challenger products. The board is available enclosed with power supply as the Model 500-1 for $429, and in an 8 slot Challenger case as the Model 500-8 for $629. For further information, contact Ohio Scientific, Hiram OH 44234. ▪

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All Prime Quality — New Parts Only

Lowest Prices — Satisfaction Guaranteed

EDGE CARD CONNECTORS:

Bifurcated Contacts. Not tin. *Gold over nickel.* 50/100 Pin (.100, 1.25, + .156 Pin spacing). Double Read out.

50/100 Altair Type — Dip Solder Pins	$4.25 ea	5 pcs	$4.00 ea
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50/100 Imsai Type with Guides	$4.50 ea	5 pcs	$4.25 ea
Imsai Guides only	$ .30/pr	5 pr	$ .25/pr

All other contacts available: Solder Eyelet, Wire Wrap, etc. *All gold.*
Many other types available: 10/20, 15/30, 18/36, etc.
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25 PIN SUBMINIATURE CONNECTORS:

Gold Plated Contacts.

DB25P Plug	$2.60 ea	5 pcs	$2.25 ea
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DB51212-1 Hood (grey)	$1.00 ea	5 pcs	$ .95 ea
DB51226-1A Hood (black)	$1.10 ea	5 pcs	$1.00 ea

SAVE:

Buy a complete set:
1 Plug, 1 Socket, 1 Hood (any) $6.50/set
5 Sets $6.25/set

2708 1KX8 PROM 450 NS
$16.75 ea
5 pcs or more $15.70 ea

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$12.00 ea
5 pcs $11.50 ea

Write for larger quantity discounts.

Dealers welcome.

Minimum order $10.00: Add $1.00 for shipping and handling. Orders over $25.00: We pay the shipping: Calif. residents add 6% tax. No COD's: For immediate shipment send money order or cashier's check.

When ordering: State method of shipment: Mail or UPS.

ORDER FROM: *Beckian Enterprises*

P.O. Box 3089 Simi, Calif. 93063

4K RAM BOARD

Assembled and tested. **$89.95**



See kit below.

4K RAM BOARD KIT

450ns Access RAMs
Fully Buffered
Low Power **$79.95**
Static
5V only
4½ x 6 inch board

Buy 4 RAM Board kits at $79.95 each and an 8 slot Mother Board is yours **FREE.**

Includes 8 connectors and card guides.

MOTHER BOARD

8 SLOT 44 PIN BUS
50 Pin Edge Connector

Mother Board $20.00 ea
Connectors 2.50 ea
Card guides for above $10.00 per set.

4K PROM BOARD

—Low Power
—5 V Only
—Industry Standard Bipolar PROM
—Compatible With Our Bus

KIT WITH 2K OF PROM $79.95

Additional 2 K of PROM $40.00

2102 — $1.20 Multiples of 25 only.
Low power, 450 n.s. Access and cycle.

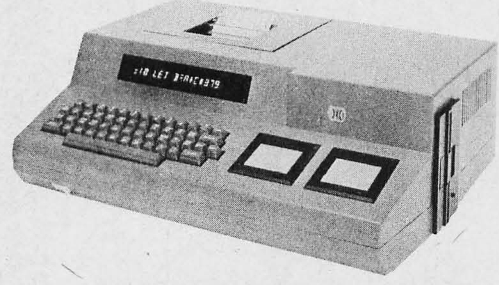
DANA 2000A Multimeter
Regularly $199.50 Our Price $165.00

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Discounts available at OEM quantities. For orders less than $25.00 total, add $1.25 for shipping. California residents add 6% sales tax. Estimated shipping time 2 days ARO with money order. For checks allows 7 days for check to clear.

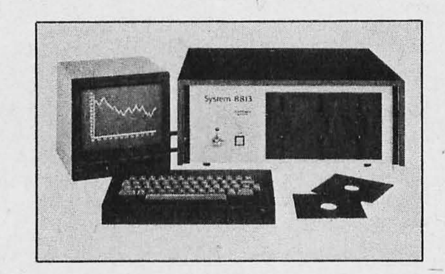
A 6800 Based Integrated System



This 6800 based system features a keyboard, 20 character alphanumeric display, 40 character per line impact printer, single or dual tape cassette drives, minifloppy disk, RS232C ports, and 9 slot card cage integrated into one case. Programmable memory expansion to 65 K bytes and 16 K byte EROM cards are also available as options. Software for the system includes a powerful 6 K byte operating and debugging system optionally available in ROM, a BASIC interpreter, FORTRAN compiler and linking loader. The ROM debugger features interactive translation of assembly language mnemonics, tape, disk and printer commands, multiple breakpoints and other functions. The system is available in two configurations: the DE68DT which includes a minifloppy disk drive, and the DE68C which fits into a smaller case without the minifloppy. Prices start at $2200 in single quantities, from Digital Electronics Corporation, 415 Peterson St, Oakland CA 94601, (415) 532-2920. ■

Circle 575 on inquiry card.

A Minifloppy Based Desk Top Personal Computer



The System 8813 is a compact complete disk based microcomputer. The central unit, no larger than a stereo component, includes 16 K bytes of programmable memory and room for three minifloppy disk drives, in a walnut case with a brushed aluminum front panel. Included in the package is a video monitor, keyboard with cable, and complete system software on diskette.

System software allows you to put the system to work immediately, running applications in either assembly language or in fully extended BASIC. The small separate keyboard permits convenient use of the system at desk or table. The high speed video display exhibits results in graphics and alphanumerics. Because it uses minifloppy disks, the 8813 allows convenient storage and fast access to programs and data by means of simple user commands. Prices for the 8813 start at $3250, from PolyMorphic Systems, 460 Ward Dr, Santa Barbara CA 93111, (805) 967-0468. ■

An F8 Based System



This system features the Mostek F8 microprocessor with a 128 byte scratch pad memory, a 1 K byte system monitor in ROM, and a memory interface with 65 K byte addressing range. The system is housed in an attractive commercial grade cabinet with a 12 slot mother board, a heavy duty 15 A power supply, 8 K bytes of programmable memory, a 20 A current loop or RS232 serial interface, and three 8 bit parallel IO ports. A 5 K BASIC interpreter is included and an 8 K BASIC and resident assembler and editor are planned. The F800 system costs $499 as a kit or $699 assembled and tested. Additional 4 K memory boards are $129 in kit form or $199 assembled and tested. Other accessory boards are planned. The F800 is available from Microdata Systems, 2 Mack Rd, #101, Woburn MA 01801, (617) 935-9870. ■

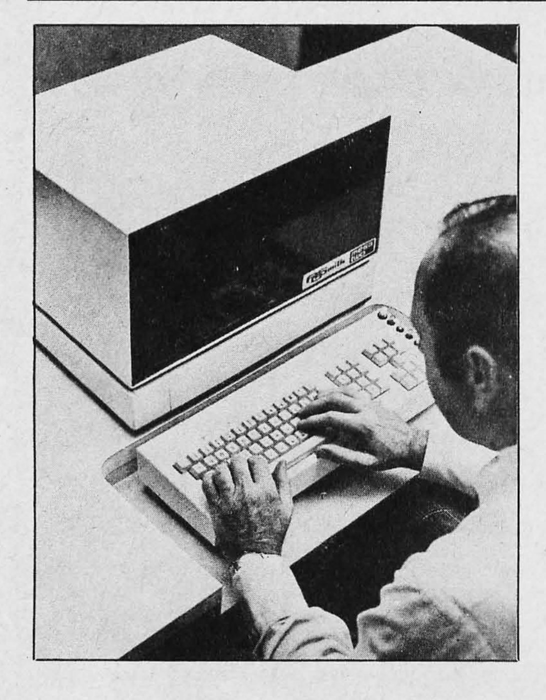
Circle 576 on inquiry card.

8080 Based System Features Front Panel Firmware



This Altair (S-100) bus compatible system uses a 12 button keyboard and a 10 digit LED display controlled by a monitor program in ROM to implement "front panel" functions such as examining and altering the contents of any register, memory location or IO device. Single step, slow step, halt, run and reset functions are also provided. The 8080A based Equinox 100 comes with a constant voltage 20 A power supply and a shielded, actively terminated 20 slot bus board. An attractive aluminum case with a smoked Plexiglas front and a key operated power switch are included in the basic system, with a swing open top, tilt up stand and carrying handle available as options. The Equinox 100, a joint venture of Parasitic Engineering and Morrow's Micro-Stuff, is available for $699 in kit form from Parasitic Engineering, POB 6314, Albany CA 94706, (415) 547-6612. ■

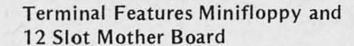
Circle 578 on inquiry card.



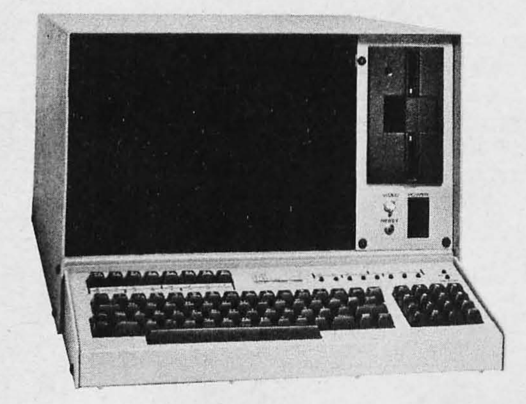
Turnkey Business System Offers Security

The Mesa Two small business computer comes complete with packaged programs for accounts receivable, accounts payable, inventory, payroll and general ledger. Designed to be operated by clerical personnel, the system features on line source data validation, passwords, and audit trails from financial statements back to source documents, providing security and management control "without the need for data processing technicians." The Mesa Two can also communicate with the manufacturer's central IBM 370 computer for larger scale applications. The system includes a processor with 64 K bytes of memory, 10 million bytes of mass storage, a keyboard and display, and a 165 character per second printer. The Mesa Two is available from A O Smith Corporation, 3533 N 27th St, Milwaukee WI 53216, (414) 447-4470. ■

Circle 577 on inquiry card.



Terminal Features Minifloppy and 12 Slot Mother Board



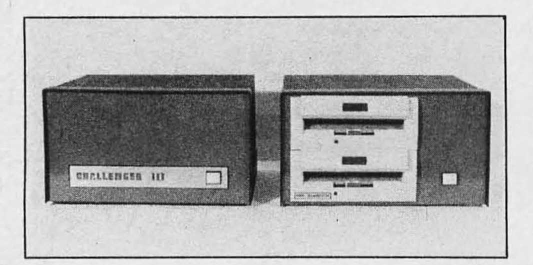
The Model MCS-PT processor terminal is a self-contained computer system with display and disk storage, a full keyboard and a 12 slot mother board. It may be used either as a stand alone processor or as a processor terminal in a larger system. Features of the MCS-PT include a 15 inch (38.0 cm) high resolution monitor, a full upper and lower case ASCII keyboard with eight user designated special function keys and a 16 key numeric cluster pad. One Shugart SA-400 Minifloppy disk drive is standard.

The 12 slot mainframe contains a CPU board that features an 8080 processor and a special circuit that implements a start up "jump to" routine to any user selected byte address. 16 K bytes of memory are provided with additional memory as an optional item. A disk controller which will handle four drives and a video board are also standard items. The IO board provides three parallel and three serial ports with selectable data rates of 75 to 19,200 bps.

The whole unit is housed in a heavy duty aluminum cabinet with power provided by a constant voltage transformer power supply. A fan, washable filter and all edge connectors and card guides are furnished. Software provided includes CP/M DOS and BASIC on disk. The MCS-PT fully assembled and tested is priced at $3495, or $2995 in kit form. The unit is also available without the disk drive and controller at $2495 assembled or $2195 in kit form. For more information contact CMC Marketing Corporation, 7231 Fondren Rd, Houston TX 77036, (713) 774-9526.■

Circle 601 on inquiry card.

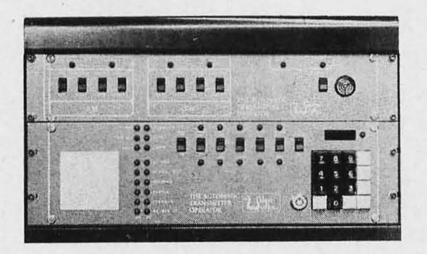
New 3 Processor System Can Run Most Published Software



The Challenger III comes equipped with three of the most popular microprocessors, the 6800, 6502 and Z-80, and hence is capable of running most published microprocessor software with appropriate modifications for memory use and input output. Optional features provide automatic switching between processors under software control and addressing of up to 1 million bytes of programmable memory. A floppy disk with the OS-65D operating system comes standard with the Challenger III, and a 74 million byte hard disk is available as an option. The Challenger III and the Model 510 board with all three microprocessors are fully compatible with other Challenger hardware and software products. The entire product line is described in a new catalog available for $1 from Ohio Scientific, 11681 Hayden St, Hiram OH 44234, (216) 569-7905.■

Circle 602 on inquiry card.

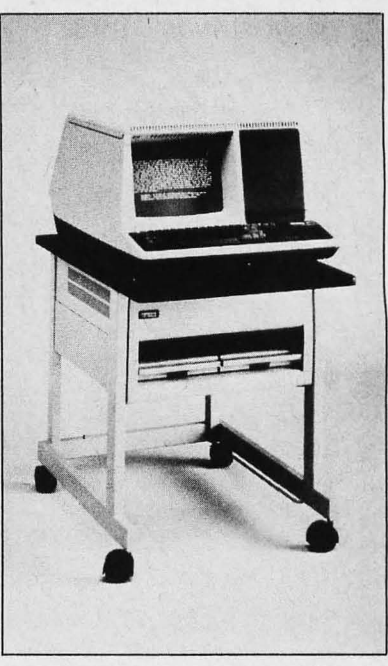
Transmitter Controller for Broadcast Stations



The problem of radio or TV broadcast station automation was discussed in Letters in the February 1977 (page 81) and May 1977 (page 105) issues of BYTE. One step is this direction is the Automatic Transmitter Operator from Widget Works Inc. This microprocessor based unit monitors and controls power, modulation, and transmitter hours of operation, eliminating the need for 3rd class licensed operators and transmitter readings. A single unit handles up to four AM or FM transmitters with proper options, and is guaranteed to meet FCC specifications for ATS control for one year from date of delivery. All hours of operation for the entire year are programmed into the unit at the time of manufacture. Calibration is performed with a calculator keyboard. Pricing varies with configuration and options, starting at $4500. For more information, contact Widget Works Inc, POB 79, Medina OH 44256, (216) 336-7500.■

Circle 603 on inquiry card.

New DECstation Employs Single Chip PDP-8



The venerable PDP-8 lives on in Digital Equipment Corporation's new DECstation, which incorporates a single chip version of the 12 bit processor. The central element of the new system is an integrated processor and display unit, the VT78, which includes a video terminal with upper and lower case ASCII characters, 16 K 12 bit words or programmable memory, a real time clock and a floppy disk interface. Five IO ports on the back of the VT78 are designed to be connected to peripherals with simple cables like those used in a component stereo system. The ports include two serial interfaces with data rates from 50 to 19,200 bps, a parallel interface for units such as printers, a floppy disk interface, and one to facilitate local input of programs. The DECstation runs under OS/78, an extended version of the PDP-8's operating system OS/8 Version III, and offers FORTRAN and BASIC compilers, the PAL-8 assembler, and various utilities. The standard DECstation configuration, which includes the VT78 and a dual drive floppy disk, is priced at $7,995. More information is available from Digital Equipment Corporation, Maynard MA 01754, (617) 897-5111, ext 3300.■

Circle 604 on inquiry card.

System, Not Peripheral

On page 252 of November 1977 BYTE, the Apple II press release was incorrectly categorized as a "peripheral." This complete computer *system* should have been placed in the "systems" category.

Our apologies to Steve Jobs and Steve Wozniak.■

What's New?

SOFTWARE

Multitasking Operating System Rivals IBM 360/91

This multiuser, multitasking operating system for 8080 and Z-80 based computers is modeled after the IBM System/360 Model 91 operating system used at the University of California, Los Angeles. It supports more than 25 user terminals with 64 K bytes of memory, and permits one user terminal to control many concurrently running tasks. Functions include block and line editing, file merging and transfer, interterminal communication, passwords and user accounting, task status reports and a system log, disk map display and print queue support. The system includes a disk based 8 K BASIC compiler which generates reentrant code. The developers claim that the system provides highly efficient resource management by maintaining dynamic, noncontiguous files, dynamically allocated memory and extensive disk buffering. The FAMOS™ system costs $1750 and must be used with a special interrupt board ($300) for the Altair (S-100) bus. The system is available from MVT Microcomputer Systems Inc, 21822 Sherman Way, Canoga Park CA 91303, (213) 348-2030.■

Circle 592 on inquiry card.

An Interactive Word Processing System

This word processing system displays your text on a video screen in the form in which it will be printed, as you enter new text or make modifications. Each line is continuously formatted and justified, and surrounding text is moved up or down as strings are inserted or replaced. Text can be reviewed by variable speed scrolling in the forward or reverse directions. Encoded strings may be used to create selective mailing lists. Line and page length and spacing can be modified as desired, and titling and page numbering is included. A version designed for the Diablo Hy-Type printer includes character spacing and bidirectional printing. "The Electric Pencil" runs on an 8080 or Z-80 based computer with 8 K bytes of memory, a Processor Technology VDM-1 or PolyMorphic Systems video interface and video monitor, a Tarbell cassette interface and cassette recorder, and a printer. The package is priced at $100 or $150 for the Diablo version, and is available at computer stores or from the author, Michael Shrayer, 3901 Los Feliz Blvd #210, Los Angeles CA 90027, (213) 665-7756.■

Circle 593 on inquiry card.

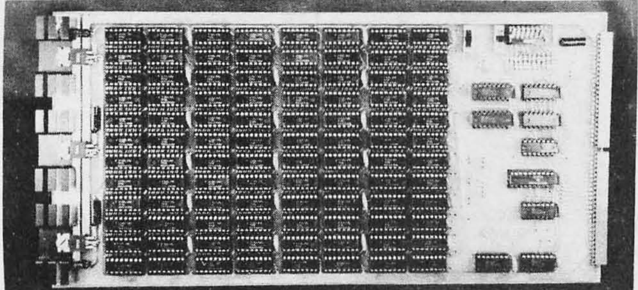
Want Z-80 Software?

Here's software for Altair (S-100) bus compatible Z-80 based systems, designed with Cromemco's ZPU processor board especially in mind. A Z-80 monitor ($25) fits in 1 K bytes of memory and allows the user to examine and modify registers and memory locations, set up to five breakpoints, program 2708 type EROMs using the Cromemco Bytesaver board, and perform other functions. The ROS Resident Operating System ($40) provides most of the monitor functions and also includes a Zilog compatible assembler and a text editor, all designed to run in 8 K bytes of memory. Control BASIC ($40), available for both 8080 and Z-80 based systems, is an extended version of Dr Wang's Palo Alto Tiny BASIC which includes input and output commands for direct IO control, ability to call user subroutines with any number of arguments, string input and output, numeric field widths and other features, yet it fits in just over 3 K bytes of memory. Included with Control BASIC is an exciting version of Star Trek "that's almost impossible to win." Wish you could run Z-80 software on your Processor Technology SOL-20? You can with the ZOL modification kit ($29.95), which lets you install a Cromemco ZPU board into the SOL's mainframe. All these goodies are available from HUH Electronic Music Productions, POB 259, Fairfax CA 94930, (415) 457-7598.■

Circle 595 on inquiry card.

Circle 42 on inquiry card.

New! ECONORAM VI™ is here—



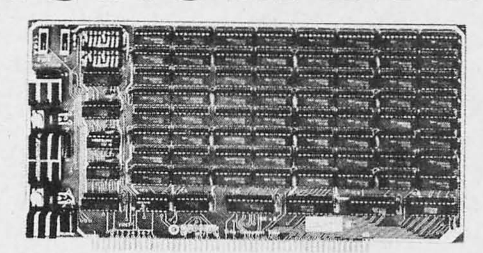
12Kx8 memory kit for the Heath H8

$235.00

We proudly welcome our newest memory board family member, designed from the ground up for full compatibility with the Heath Company H8. Organized as two independent blocks for flexibility: one 8K block (locatable on any 8K boundary) and one 4K block locatable on any 4K boundary. Has the same basic features of our ECONORAM II™— all static design, dipswitch address selection, switch selected write protect and phantom, sockets for all ICs, full buffering—plus the required hardware and edge connector to mate mechanically with the H8. Now you can have our 12K board for the price of the Heath Company's 8K ... with the performance you've come to expect from products carrying the ECONORAM™ name.

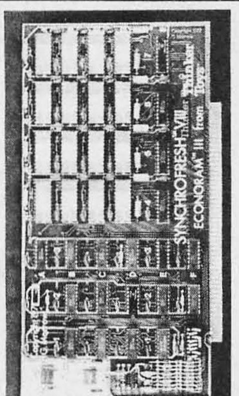
Also available: H8 4K to 8K conversion kit ($90). If you have a Heath Company 4K memory, plug in these ICs and you'll have a full 8K. Kit includes eight TI4044 memories and matching sockets.

ECONORAM II™



This 8K x 8 static memory is a consistent winner, whether you plug into an Altair, IMSAI, or any other S-100 buss computer. Configured as two independent 4K blocks, with separate protect for each block and vector interrupt provision if you try to write into protected memory. Handles DMA devices. All address and data lines fully buffered. Tri-state outputs for use with bi-directional busses. Selectable write strobe (writes on either $\overline{PWR}$ or MWRITE), and dipswitch selectable address. We guarantee 450 ns speed, although many users report running this board in conjunction with 4 MHz Z-80s without using the on board wait state provison. The mechanical quality matches the design, with gold-plated edge fingers, legended and solder masked board, sockets for all ICs, and industrial grade or better components. Join the thousands who have made this our most popular computer board!

Kit form.. $130
Assembled, tested, 1 year warranty............................ $150
Special! Four ECONORAM II™ kits........................... 4/$475



new and dynamic: ECONORAM III™

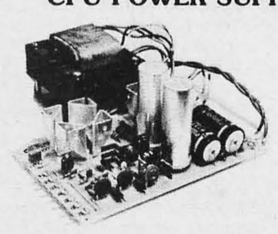
Here is the first 8K x 8 dynamic RAM that performs well enough to merit the ECONORAM™ name. Thanks to the SynchroFresh* timing process, refresh fits naturally into the timing of the S-100 buss ... now you can have half the power of statics, but without the traditional timing hassles you've come to associate with dynamic memories.

In addition to low power, this board runs at zero wait states with an 8080 CPU, and is configured as two separate blocks for maximum versatility. Not a kit: shipped assembled, tested and ready to plug into any S-100 buss computer (Altair, IMSAI, etc.). 1 year warranty.

Assembled 8K x 8 ECONORAM III™ $149.00

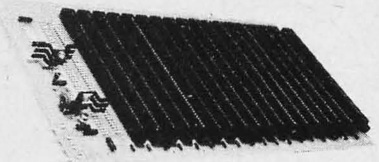
*SynchroFresh is a trade mark of Thinker Toys

CPU POWER SUPPLY ($50)



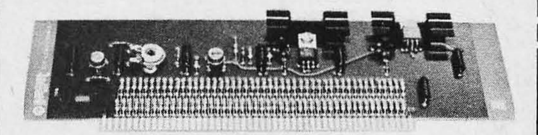
Gives a full 5V at 4A with crowbar overvoltage protection, along with +12V at ½A, -12V at ½A, and adjustable bias supply (5 to 10V at 10 mA). Although intended for use with small computer systems, this is also an excellent supply for bench and development work.

10 SLOT MOTHERBOARD ($90; 18 SLOTS $124)



Add one of these on to an existing S-100 system, or use as the nucleus of a stand-alone system. Both kits come with all edge connectors and include on-board active, regulated terminations to minimize crosstalk, overshoot, ringing, and other glitches that can occur with unterminated lines. Includes lots of bypass caps and heavy power traces.

ACTIVE TERMINATOR ($29.50)



Plug this board into any S-100 motherboard to clean up the problems associated with unterminated lines. Uses the same circuitry as our Motherboards.

TERMS: Please allow up to 5% for shipping; excess refunded. Californians add tax. COD orders accepted with street address for UPS. For VISA® /Mastercharge® orders call our 24 hour order desk at **(415) 562-0636.** Prices good through cover month of magazine.



FREE FLYER: These are just a few of the items we carry for the computer enthusiast. We also stock a broad line of semiconductors, passive components, and hobbyist items. We will gladly send you a flyer describing our products upon receipt of your name and address.

Extended Monitor for the KIM-1

"XIM" (Extended IO Monitor) is a programming and debugging package for the KIM-1 computer. It provides commands to move, compare or search blocks of memory, set break points, calculate branch displacements, load ASCII characters and dump hexadecimal data, and display the processor registers. "XIM" occupies just under 1 K bytes of memory and is easily relocated. A 45 page user's manual with source listing is included, with object code on paper tape for $10 or on KIM-1 cassette for $12, from Pyramid Data Systems, 6 Terrace Av, New Egypt NJ 08533.■

Circle 594 on inquiry card.

A New 8080 Assembly Language Debugger

The Dynamic Debugger is a diagnostic program for 8080 assembly language which has been announced by Computer Mart of New Jersey. The program features an automatic breakpoint mode to facilitate debugging. The price is $30 on paper tape or cassette, or $35 on diskette from the Computer Mart of New Jersey, 501 Route 27, Iselin NJ 08830, (201) 283-0600.■

Circle 596 on inquiry card.

A New BASIC Compiler

Software Dynamics is offering a new BASIC compiler said to feature floating point arithmetic, subscripting, formatted output and character string manipulation. The compiler requires 16 K bytes of programmable memory space. The price of the compiler is $150, and the manual sells for $10. For more information, contact Software Dynamics, 17914 Laurelbrook Pl, Cerritos CA 90701, (213) 962-6492.■

Circle 598 on inquiry card.

Extensions to Processor Technology Software Package #1

Software Package 0.5 is a set of extensions to Processor Technology's Software Package #1 (a basic assembler, editor and operating system for the 8080). New features include automatic insertion and reordering of line numbers, commands to find and change or insert strings, and an efficient tape driver for Tarbell or DaJen cassette interfaces. Complete source code is supplied for $14.95, with object code on paper tape for $19.95 or on Tarbell tape for $24.95, from Objective Design Inc, POB 20325, Tallahassee FL 32304.■

Circle 597 on inquiry card.

Real Time Warfare Game

Encounter! is a game that exploits the real time response capabilities of a computer. Unlike most board games, there is no taking turns between two players; each player attacks and defends as many places on the field as he is mentally able to maintain. Parameters such as the speed of play, configuration of the playing field, location of "home" and "blocked" districts, "birthrate" of new men, and the game time limit can be altered at will. Encounter! is designed for an Altair (S-100) 8080 or Z-80 based system with a Processor Technology VDM-1 and two ASCII keyboards. Complete source code is provided, with paper tape for $16.95 or with Tarbell tape for $19.95, from Objective Design Inc, POB 20325, Tallahassee FL 32304.■

Circle 599 on inquiry card.

An IBM 1130 Simulator for Nova Computers

Icon Corporation has announced its new ELLIPSE 1130 processing system designed to simulate the IBM 1130 on a Data General Nova computer. This makes available a wide variety of COBOL, APL, RPG, FORTRAN IV and other types of programs to the Nova user with no modifications needed. Contact Icon Corporation, 11300 Rockville Pike, Suite 10 NE, Rockville MD 20852, (301) 770-1885.■

Circle 600 on inquiry card.

What's New?

PUBLICATIONS

New Micro Store Catalog



This 36 page catalog describes the offerings of the two Micro Stores in Richardson and Arlington TX. Like a few other recent computer store catalogs and shopping guides, this one helps educate the customer by including a section on "How to Buy a Microcomputer" and by providing extensive product descriptions (as many as five pages on one manufacturer's product line). The catalog is available from the Micro Store, 634 S Central Expy, Richardson TX 75080, (214) 231-1096.■

Circle 609 on inquiry card.

A Marketing Resources Catalog

A free catalog listing publications and services related to the techniques of marketing electronic products is being offered by Mainly Marketing. The manuals and services listed are aimed at engineers, manufacturers' representatives, marketing and sales people, and advertising people. A monthly newsletter is also described which deals with this field. To receive the catalog, send a large stamped (24¢) self-addressed envelope to Schoonmaker Associates, Drawer M, Coram NY 11727.■

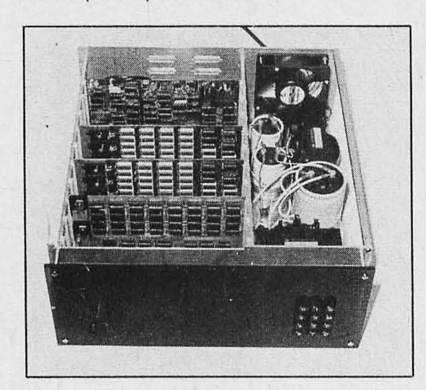
Circle 610 on inquiry card.

The Story of Magnetic Media

Want to know more about the future potential of removable magnetic storage devices and media? A new six page brochure reviews the history of removable media and discusses current and future applications. Copies are free from Information Terminals Corp, 323 Soquel Way, Sunnyvale CA 94086.■

Circle 606 on inquiry card.

Want to Build Your Own Altair (S-100) Card Frame?



The Crate Information Packet is a complete set of plans for constructing an Altair (S-100) compatible card frame and power supply. The design can be adapted to any of the available Altair (S-100) mother boards, and can be built from commonly available materials for about $150. The plans include information on sources of materials, tools, parts for the power supply, and front panel options. Either a full size or a twelve slot card frame can be built. The information packet is $19.95; also available are prepunched and drilled front and rear panels for $11.95 each or $20 per set, from Objective Design Inc, POB 20325, Tallahassee FL 32304.■

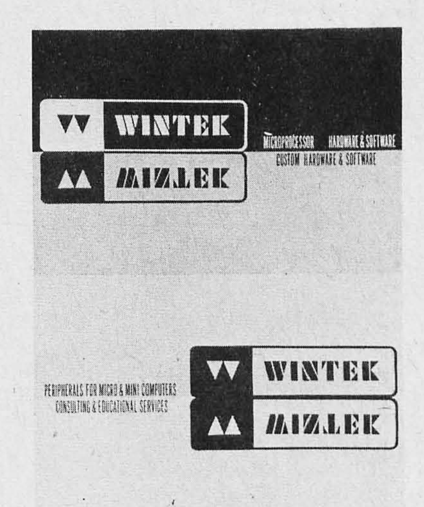
Circle 611 on inquiry card.

User Manual Available for BASIC-E

Users of the BASIC-E compiler on the CP/M operating system for 8080 based computers will profit from this excellent, 200 page reference manual and user's guide. It goes far beyond most BASIC manuals and indeed beyond most textbooks on BASIC programming. Besides its comprehensive coverage of BASIC language features, including character string handling and disk file definition and access, the manual provides information on interaction with the user's terminal in BASIC, compiler options and error codes, a guide for beginners, and hints on problem solving and programming techniques. 16 appendices offer examples of BASIC-E programs and treat topics such as how a program works, compilers versus interpreters and structured programming techniques. The manual itself is priced at only $15, while a floppy disk containing the latest BASIC-E compiler and runtime monitor, a formatting procedure, letter writer and name file manager, a file transfer facility for object files, and miscellaneous other programs sells for $60, from John K Jacobs, JEM Company, 2555 Leavenworth St, Suite 301, San Francisco CA 94133, (415) 673-8962.■

Circle 612 on inquiry card.

New Catalog from Wintek



This catalog describes the hardware, software and custom services available from Wintek Corporation, including the WINCE 6800 series micromodules, software such as the PL/W high level language, relocating linker and BASIC, consulting, and in-house courses on microprocessors. The catalog is available from Wintek Corporation, 902 N 9th St, Lafayette IN 47904, (317) 742-6802.■

Circle 605 on inquiry card.

Datapro Report on Microcomputers

This new 36 page report provides detailed specifications on 144 models of microcomputers, and comments on their potential applications. The report distinguishes between original equipment manufacturer (OEM) microcomputers, micro development systems and hobbyist microcomputers, and evaluates products in each category. Offerings from 57 vendors are covered, and names and addresses of vendors are included. Reprinted from the June supplement to *Datapro Reports on Minicomputers*, the new report is available for $12 per copy from Datapro Research Corp, 1805 Underwood Blvd, Delran NJ 08075, (609) 764-0100.■

Circle 608 on inquiry card.

Manuals for Floppy Disk Controller Chip

These two manuals describe how to use the NEC uPD372 floppy disk controller chip, which provides most of the functions needed to control up to four full size or minifloppy disk drives (see "What's New?" March 1977 BYTE, page 105). Complete assembly language listings, schematics for host processor connections, timing diagrams and narrative text are included. The 70 page manual for the full size floppy drive and the 44 page manual for the minifloppy drive are $10 each from NEC Microcomputers Inc, 5 Militia Dr, Lexington MA 02173, (617) 862-6410.■

Circle 607 on inquiry card.

MICROCOMPUTER

MICROPROCESSOR's

F-8	19.95
Z-80	25.00
Z-80A	35.00
CDP1802CD	24.95
AM2901	22.95
6502	12.95
6800	19.95
8008-1	8.75
8080A	15.95
TMS-9900TL	89.95

6800 SUPPORT

6810P	4.95
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6860P	14.95
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Z80 SUPPORT DEVICES

3881	12.95
3882	12.95

F-8 SUPPORT DEVICES

3851	14.95
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2107A	3.75
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MM5270	5.00
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2513 UP	6.75
2513 DOWN	6.75
2513 UP (5v)	9.95
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MCM6571	10.80
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MCM6574	14.75
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1702A	5.00
2704	15.00
2708	20.00
2716	38.00
3601	4.50
5203AQ	4.00
5204AQ	6.00
6834	16.95
6834-1	14.95
82S23B	4.00
82S129B	4.25
8223B	2.70

8080A SUPPORT DEVICES

8212	3.95
8214	9.95
8216	4.50
8224	4.95
8228	8.75
8238	8.00
8251	12.00
8253	28.00
8255	12.00
8257	25.00
8259	25.00

STATIC RAMS	1-24	25-99	100
21L02 (450)	1.50	1.40	1.25
21L02 (250)	1.95	1.80	1.50
21L11	4.25	4.10	3.95
1101A	1.49	1.29	1.10
2101-1	2.95	2.75	2.60
2102	1.25	1.15	1.00
2102-1	1.50	1.30	1.15
2111-1	4.00	3.50	3.25
2112-1	3.00	2.80	2.69
2114	17.95	16.95	16.50
31L01	2.50	2.35	2.00
3107	3.95	3.70	3.25
4200A	12.95	12.50	11.95
4804/2114	17.95	16.95	16.50
5101C-E	11.95	11.25	10.25
74C89	3.25	3.05	2.85
74S201	4.50	4.30	4.25
7489	2.25	2.10	1.90
8599	1.88	1.75	1.60
9102BPC	1.65	1.45	1.30

KEYBOARD CHIPS

AY5-2376	13.95
AY5-3600	13.95

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AY5-1014A	8.95
TR-1602A	5.50
TMS-6011	6.95
IM-6402	10.80
IM-6403	10.80

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1771B	55.95
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2518B	3.95
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TMS3002	1.00
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6520	9.00
6522	9.25
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6530-004	15.95
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USRT

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MC4024	2.50
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TV Game Chip

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Now Only $10.95

PerSci DISK AND CONTROLLER

Use the PerSci Disk and Controller now with the Info 2000 Adapter for the S-100 Bus.

INFO 2000 "SPECIAL" (includes Model 277 Dual Drive, Model 1070 Controller, Case with power supply and fan, and cable)	$2,150
Model 277 Dual Diskette Drive	$1,130
Model 1070 Controller	$740
Slimline case with power supply and fan	$280
Adapter for the S-100 Bus (Kit)	$120

JADE PARALLEL/SERIAL INTERFACE KIT
$124.95 KIT

JADE VIDEO INTERFACE KIT
$89.95 KIT

8K STATIC RAM BOARD

ASSEMBLED & TESTED

250ns.	$199.95
350ns.	$189.95
450ns.	$169.95

* WILL WORK WITH NO FRONT PANEL
* FULL DOCUMENTATION
* FULLY BUFFERED
* S100 DESIGN
* ADEQUATELY BYPASSED
* LOW POWER SCHOTTKY SUPPORT IC'S

KIT

250ns.	$169.95
350ns.	$139.95
450ns.	$129.95

IMSAI/ALTAIR **S-100** COMPATIBLE

JADE Z80 KIT

—with PROVISIONS for ONBOARD 2708 and POWER ON JUMP

$135.00 EA. (2MHZ)

$149.95 EA. (4MHZ)

BARE BOARD **$35.00**

IMSAI/ALTAIR **S-100** COMPATIBLE

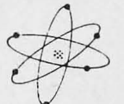
JADE 8080A KIT

– WITH EIGHT LEVEL VECTOR INTERRUPT

$110.00 KIT

BARE BOARD **$35.00**

JADE



Computer Products

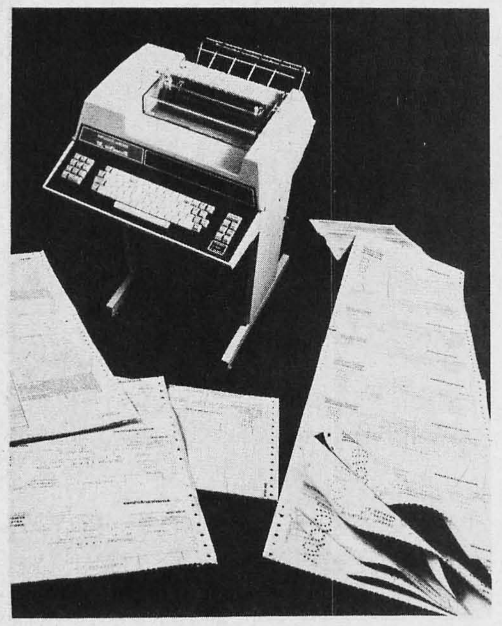
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Discounts available at OEM quantities. Add $1.25 for shipping. California residents add 6% sales tax.

CATALOG FREE WITH $10.00 ORDER

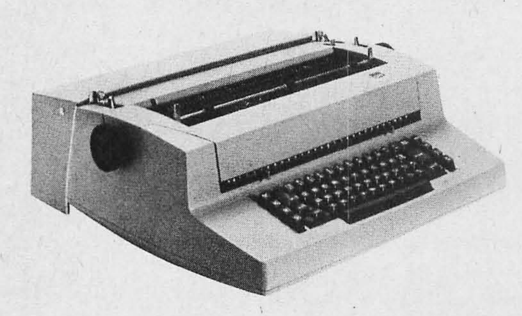
Print 9 Part Forms



Multiple forms of up to nine parts, such as airline tickets, invoices and warehousing slips, can be handled by this terminal. The Terminet Multi-Form Printer (MFP) prints 80 or 132 characters per line on 8.5 by 11 inch (21.6 by 27.9 cm) paper at 30 characters per second. Other options include magnetic or paper tape and TWX Direct Distance Dial (DDD) capability. The MFP is $1675 with 30 to 60 days delivery, or $3220 with a single magnetic cassette drive, from General Electric Data Communications Dept, AS&P, Waynesboro VA 22980, (703) 942-8161. ▪

Circle 581 on inquiry card.

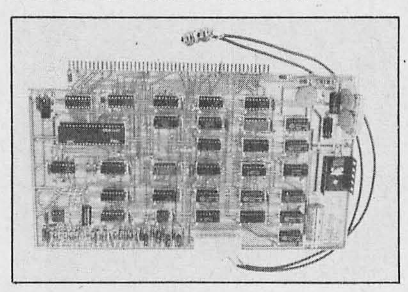
Selectric Terminal Features Microprocessor



This device uses a built-in microprocessor to make a Selectric typewriter behave like a standard ASCII terminal. It offers an RS232 interface and is fully buffered, with switch selectable data rates of 110, 134.5, 150 and 300 bps. When off line the terminal can be used as a standard office typewriter. Since the terminal employs a microprocessor it can be modified to meet special interfacing requirements, and is available with two empty card slots for user supplied interface circuits. The unit is priced at $2125 in single quantities with 60 day delivery; attractive OEM discount schedules are also available, from CPT Corporation, 1001 S 2nd St, Hopkins MN 55343, (612) 935-0381. ▪

Circle 582 on inquiry card.

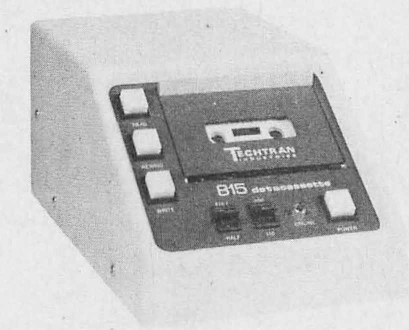
Cassette Interface for Altair 680b



This board provides an audio cassette interface using the Kansas City recording standard for the MITS Altair 680b computer. The board includes a digital demodulator and a motor control circuit for starting and stopping tape motion. Complete documentation including test point waveforms is provided. Altair 680b BASIC Version 1.2 provides facilities for saving and loading software using the cassette interface, and is available on an audio cassette. The 680b KCACR is available from MITS, 2450 Alamo SE, Albuquerque NM 87106. ▪

Circle 585 on inquiry card.

Cassette Storage for Terminals



This tape cassette drive is designed to operate with terminals and data collection devices. It offers an RS232C interface running at 110 or 300 bps. The Model 815 Datacassette weighs only 6 pounds (2.7 kg) and is priced at $950. A battery operated model, weighing 10 pounds, (4.5 kg) is priced at $1095. Delivery time is 45 days, from Techtran Industries Inc, 200 Commerce Dr, Rochester NY 14623, (716) 334-9640. ▪

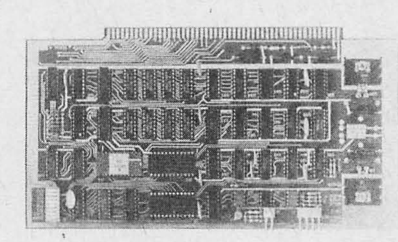
Circle 586 on inquiry card.

Experiment with This Keyboard

This user definable keyboard is ideal for the experimenter who wants to use the full APL character set, a special notation for music, or something more exotic. 100 keys are included with hot stamped letters, and 90 keys may be encoded by the user into any configuration of eight bits. Or, some keys may be used as separate switch closures to control external circuitry. Ten keys are used to directly control the eight encoding bits. Facilities are included for shifting character codes (as between upper and lower case), an electronic shift lock, and positive and negative strobe signals. Eight LEDs are provided for display of the encoding bits, and 12 additional LEDs can be used for status display. The keyboard can be configured to transmit the full 128 character ASCII set with 25 keys left over for special functions. All decoding is done with a diode matrix. The keyboard is available from Computer Electronics Inc, Box 4386, 37 Joseph Ct, San Rafael CA 94903, (415) 472-2425. ▪

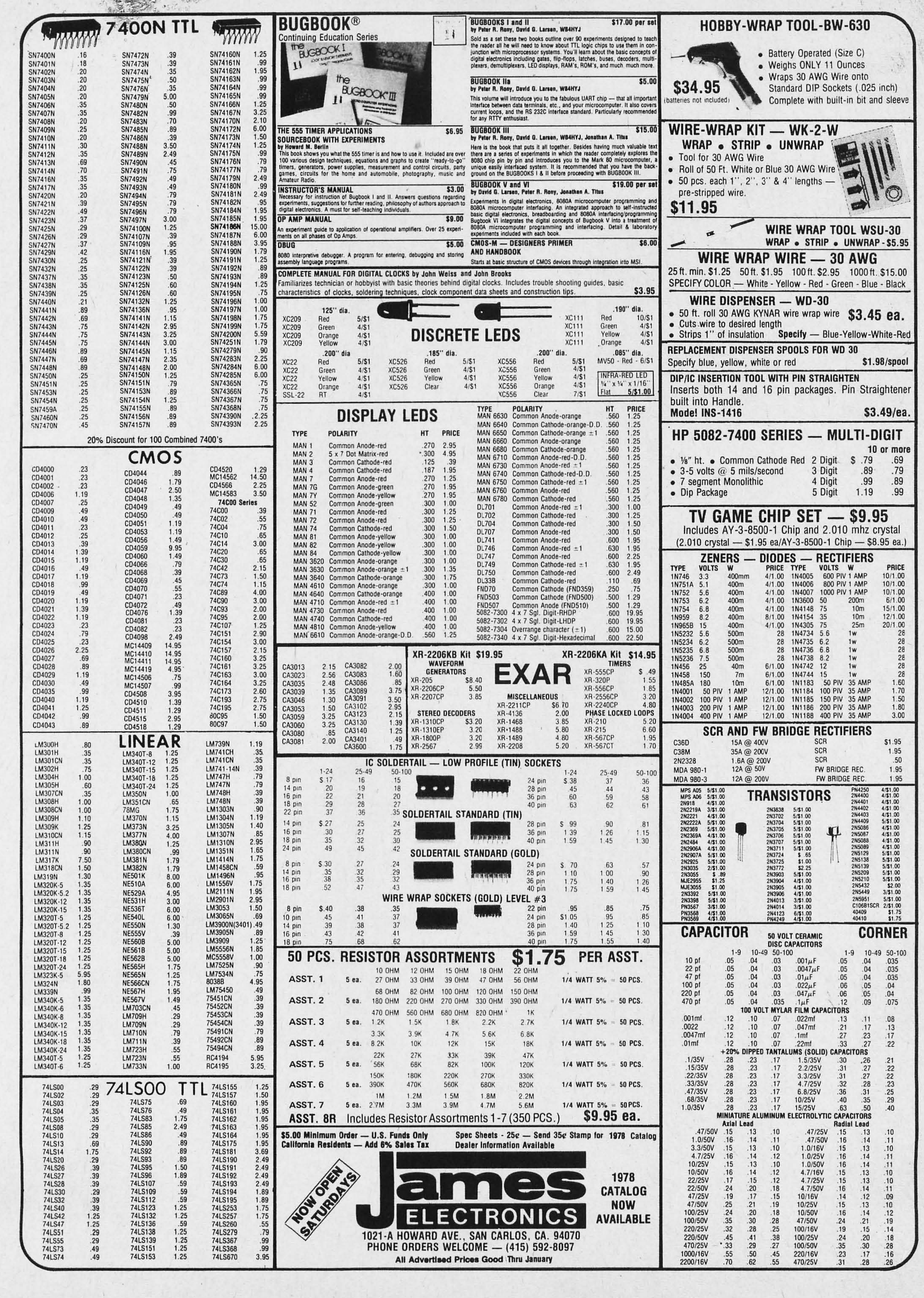
Circle 583 on inquiry card.

Versatile Video Memory Board



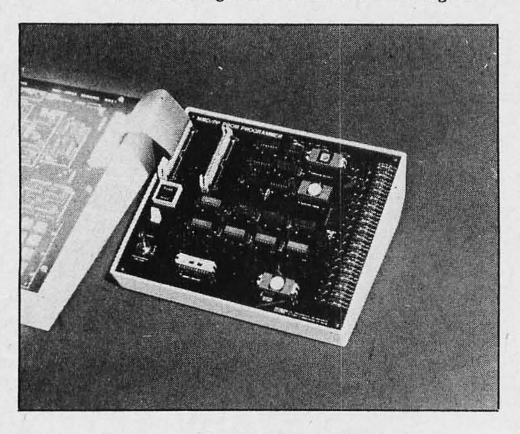
The Solid State Music VB1 video interface board for the Altair (S-100) bus offers 16 lines of 32 or 64 characters, upper case, lower case and Greek letters, video inversion (black on white or white on black), and 128 by 48 graphics. Software is included for cursor control, scrolling and graphics display. Output of the board can be parallel or composite video, suitable for a video monitor. The VB1 is $189.95 as a kit or $264.95 assembled and tested from Solid State Music, 2102A Walsh Av, Santa Clara CA 95050, (408) 246-2707. ▪

Circle 584 on inquiry card.



Circle 55 on inquiry card.

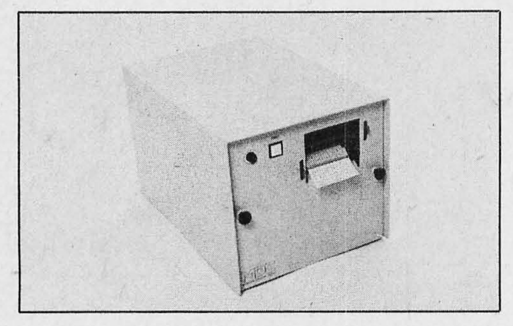
EROM Programmer for Micro Designer



This accessory for the Mini-Micro Designer (MMD-1) microcomputer trainer makes it possible to program a 256 byte 1702A erasable read only memory (EROM) in about 4 minutes. Programming data can be obtained from any block of memory in the MMD-1 or from a master EROM which is to be copied. After programming, the contents of the EROM can be verified against the source data. The programmer is attached to the MMD-1 through an included 40 pin connector and ribbon cable assembly. The MMD-PP programmer is $166 in kit form or $222 assembled, from E & L Instruments Inc, 61 First St, Derby CT 06418, (203) 735-8774. ■

Circle 588 on inquiry card.

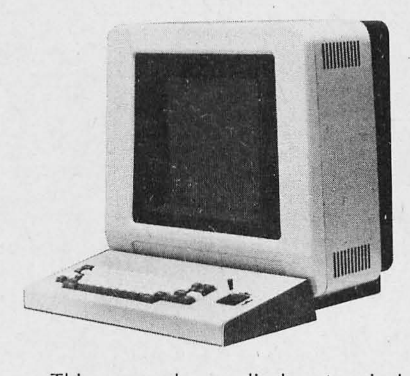
Instrumentation Printer Offers Serial Interface



This unit prints up to 21 columns of numeric and limited alphabetic data at a rate of 3 lines per second. The printing mechanism has a 5 million line life and uses a cassette loaded ink ribbon. Options include a date and time clock, event counter and paper low indicator. RS232 and 20 mA current loop interfaces simplify connection to a microprocessor. The MDC 300 printer starts at $595 in single quantities from Master Digital Corporation, 1308-F Logan Av, Costa Mesa CA 92626, (714) 751-8271. ■

Circle 589 on inquiry card.

New Plasma Display Terminal



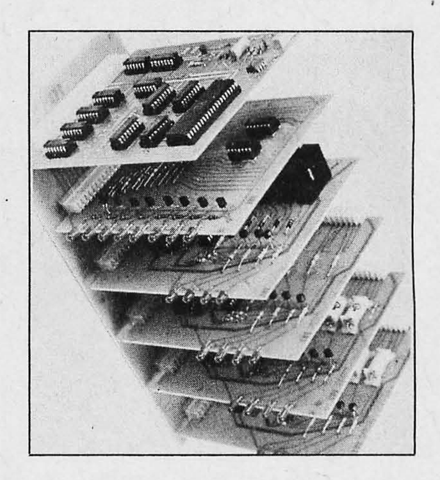
This new plasma display terminal is designed to compete with ruggedized alphanumeric and graphic cathode ray tube (CRT) terminals in the $8,000 to $15,000 price range. The plasma display features a neon orange color twice as bright as a CRT screen, with a 20 to 1 contrast ratio. The flat display plate eliminates distortion and allows a wide viewing angle, while the 50,000 Hz "refresh" sustaining voltage produces a flicker free display fixed in place by the matrix of lines "printed" on the glass plates, with a resolution equivalent to that of a 60 mesh halftone screen. The display panel itself is only a half inch deep, and it can be combined with back projection techniques to produce a display partly from film and partly from the computer, or "drawn" by the operator.

The plasma display panel consists of two glass plates printed with parallel conductor lines at right angles to each other. The space between the plates is filled with neon gas, and an oscillating voltage is applied across the gap, just below the threshold required to ionize the gas. When voltages are applied across two intersecting lines, a glowing plasma path is established at the point of intersection and thereafter sustained by the oscillating voltage. The neon "dot" can be selectively erased by dropping the voltage across the intersecting lines below the sustaining level. This selective erasing capability makes the plasma display especially suitable for real time animation.

Developed at the University of Illinois as part of the PLATO computer aided instruction system, plasma display panels are now produced by several manufacturers in the US and abroad. The Model PD 2000 terminal (pictured) incorporates the plasma panel in a commercial terminal design. Also offered are the PD 1000 and the PD 3000, the latter designed for airborne or shipboard environments. The terminals are available from Interstate Electronics Corporation, 707 E Vermont Av, POB 3117, Anaheim CA 92803, (714) 772-2811. ■

Circle 587 on inquiry card.

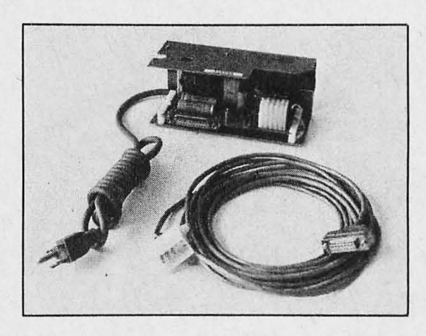
Control 128 Devices from One Port



This interface system allows you to control up to 128 separate devices or circuits through one 8 bit port or an ASCII serial interface. Devices controlled may include room lights, sprinkler systems or laboratory experiments. The system consists of a mother board and a series of interface boards, with LEDs to display the status of each board and the 8 bit bus. An enclosure is available which allows all of the LEDs to show through a red Plexiglas front panel. The XPRES interface system is available from CRC Engineering Inc, POB 6263, Bellevue WA 98007, (206) 885-7038. ■

Circle 590 on inquiry card.

Add a Cassette or Plotter to Your Teletype



This adapter provides an auxiliary input output port on a Model 33 Teletype, making it possible to add a tape cassette, XY plotter, or other device to the Teleprinter system. The adapter also works with the Teletype in local mode. The unit mounts in the pedestal of the Teletype and provides an RS232 interface terminating in a DB25S receptacle for the auxiliary equipment. Priced at $110, the adapter is available as catalog number 312 A 0566-10 from United Data Services Company Inc, 3024 N 33rd Dr, Phoenix AZ 85017, (602) 269-2449. ■

Circle 591 on inquiry card.

BREAD BOARD JUMPER WIRE KIT



Each kit contains 350 wires cut to 14 different lengths from 0.1" to 5.0'.

Each wire is stripped and the leads are bent 90° for easy insertion.

Wire length is classified by color coding.

All wire is solid tinned 22 gauge with PVC insulation.

The wires come packed in a convenient plastic box.

JK1 . . . .$10.00 / kit

SOCKET JUMPERS

Mates with two rows of .025" sq. or dia. posts on patterns of .100" centers and shielded receptacles. Probe access holes in back. Choice of 6" or 18" length.

Part No.	No. of Contacts	Length	Price
924003-18R	26	18"	$ 5.38 ea.
924003-06R	26	6"	4.78 ea.
924005-18R	40	18"	8.27 ea.
924005-06R	40	6"	7.33 ea.
924006-18R	50	18"	10.31 ea.
924006-06R	50	6"	9.15 ea.

JUMPER HEADERS

Solder to PC boards for instant plug-in access via socket-connector jumpers. .025" sq. posts. Choice of straight or right angle.

Part No.	No. of Posts	Angle	Price
923863-R	26	straight	$1.28 ea.
923873-R	26	right angle	1.52 ea.
923865-R	40	straight	1.94 ea.
923875-R	40	right angle	2.30 ea.
923866-R	50	straight	2.36 ea.
923876-R	50	right angle	2.82 ea.

INTRA-CONNECTOR

Provides both straight and right angle functions. Mates with standard .10" x .10" dual row connectors (i.e. 3m, Ainsley, etc.) Permits quick testing of inaccessible lines.

Part No.: 922576-26 **No. of contacts:** 26 **Price** $6.90 ea.

INTRA-SWITCH

Permits instant line-by-line switching for diagnostic or QA testing. Switches actuated with pencil or probe tip. Mates with standard .10" x .10" dual-row connectors. Low profile design. Switch buttons recessed to eliminate accidental switching.

Part No.: IS-26 **No. of contacts:** 26 **Price** $13.80 ea.

CRYSTALS

THESE FREQUENCIES ONLY

Part #	Frequency	Case/Style	Price
CY1A	1.000 MHz	HC33/U	$5.95
CY2A	2.000 MHz	HC33/U	$5.95
CY2.01	2.010 MHz	HC33/U	$1.95
CY3A	4.000 MHz	HC18/U	$4.95
CY7A	5.000 MHz	HC18/U	$4.95
CY12A	10.000 MHz	HC18/U	$4.95
CY14A	14.31818 MHz	HC18U	$4.95
CY19A	18.000 MHz	HC18/U	$4.95
CY22A	20.000 MHz	HC18/U	$4.95
CY30B	32.000 MHz	HC18/U	$4.95

CONNECTORS

PRINTED CIRCUIT EDGE-CARD

.156 Spacing-Tin-Double Read-Out

Bifurcated Contacts — Fits .054 to .070 P.C. Cards

15/30	PINS (Solder Eyelet)	$1.95
18/36	PINS (Solder Eyelet)	$2.49
22/44	PINS (Solder Eyelet)	$2.95
50/100	PINS (Wire Wrap)	$6.95
50/100A (.100 Spacing)	PINS (Wire Wrap)	$6.95

25 PIN-D SUBMINIATURE (RS232)

DB25P	PLUG	$3.25
DB25S	SOCKET	$4.95

205-CB HEAT SINKS 680-.75A

205-CB	Beryllium Copper w-black finish for T0-5	$ .25
291-.36H	Aluminum for T0-220 Transistors & Regulators	$ .25
680-.75A	Black Anodized Aluminum for T0-3	$1.60
Dude 4	Black Anodized Aluminum — predrilled mounting holes for T0-3 — 4¾ x 1¼ x 2"	$1.75

Etching Kits (cannot be shipped via air)

32 X A-1	P.C. Etch Materials Kit enough for 5 circuit boards	$29.95 ea.
27 X A-1	Etched Circuit Kit Complete kit — only add water	$ 9.95 ea.

Plugboards

3662	6.5 X 4.5 X 1/16 Epoxy glass P-Pattern-44 P.C. Tabs-spaced .156"	$ 6.95 ea.
22/44	Mating connector for plugboard — 22 pin double readout	$ 2.95 ea.
8800V	Universal Microcomputer/Processor plugboard — Epoxy Glass — complete with heatsink and mounting hardware 5.313 X 10 X 1/16 copper clad	$19.95 ea.

Vector

1/16 VECTOR BOARD

	0.1" Hole Spacing Part No	P-Pattern L	P-Pattern W	Price 1-9	Price 10 up
PHENOLIC	64P44 062XXXP	4.50	6.50	1.72	1.54
	169P44 062XXXP	4.50	17.00	3.69	3.32
EPOXY GLASS	64P44 062WE	4.50	6.50	2.07	1.86
	84P44 062WE	4.50	8.50	2.56	2.31
	169P44 062WE	4.50	17.00	5.04	4.53
	169P84 062WE	8.50	17.00	9.23	8.26
EPOXY GLASS COPPER CLAD	169P44 062WEC1	4.50	17.00	6.80	6.12

63 KEY KEYBOARD $29.95

This keyboard features 63 unencoded SPST keys, unattached to any kind of P.C.B. A very solid molded plastic 13" x 4" base suits most applications.

HD0165	Encoder Chip (encodes 16 Keys)	$7.95 ea.
AY-5-2376	Encoder Chip (encodes 88 Keys)	$14.95 ea.

MICROPROCESSOR COMPONENTS

8080A	CPU	$16.00	CDP1802	CPU	$19.95
8212	8 Bit Input/Output	4.95	MC6800	8 Bit MPU	24.95
8214	Priority Interrupt Control	15.95	MC6820	Periph. Interface Adapter	15.00
8216	Bi-Directional Bus Driver	6.95	MC6810AP1	128 x 8 Static RAM	6.00
8224	Clock Generator/Driver	9.95	MC6830L8	1024 x 8 Bit ROM	15.00
8228	System Controller Bus Driver	10.95	Z80	CPU	29.95

CPU'S

8080A	Super 8008	16.00
2650	8 BIT MPU	26.50
P8085	CPU	29.95

SR'S

2504	1024 Dynamic	$ 3.95
2518	Hex 32 BIT	7.00
2519	Hex 40 BIT	4.00
2522	Dual 132 Bit SSR	2.95
2524	512 Dynamic	1.95
2525	1024 Dynamic	3.00
2527	Dual 256 BIT	3.95
2529	Dual 512 BIT	4.00
2532	Quad 80 BIT	3.95
2533	1024 Static	5.95
3341	Fifo	6.95
74LS670	16 x 4 Reg	3.95

UART'S

AY-5-1013	30K Baud	$5.95

ROM'S

2513(2140)	Char. Gen.-upper case	$ 9.95
2513(3021)	Char. Gen.-lower case	9.95
2516	Char. Gen.	10.95
MM5230	2048 BIT (512 x 4 on 256 x 8)	1,95

RAM'S

1101	256 x 1	Static	$ 1.49
2101	256 x 4	Static	5.95
2102	1024 x 1	Static	1.75
2107/5280	4096 x 1	Dynamic	4.95
2111	256 x 4	Static	6.95
7489	16 x 4	Static	2.49
8101	256 x 4	Static	5.95
8111	256 x 4	Static	6.95
8599	16 x 4	Static	3.49
21L02/91L02	1024 x 1	Static	2.25
74200	256 x 1	Static	6.95
93421	256 x 1	Static	2.95
MM5262	2K x 1	Dynamic	2 for 1.00
UPD414(2104)4K		Dynamic 16 Pin	5.95

PROMS

1702A	2048	Famos	$ 9.95
5203	2048	Famos	14.95
82S23	32 x 8	Open C	5.00
82S123	32 x 8	Tristate	5.00
74S287	1024	Static	7.95
3601	256 x 4	Fast	3.95
2708	8K	Eprom	19.95
2716	16K	Eprom	34.95
6301-1	1024	Tri-State Bipolar	3.49
6330-1	256	Open Collector Bipolar	2.95

SPECIAL REQUESTED ITEMS

FCM3817	$5.00	11C90	19.95	7205	19.95	9368	3.95
AY-3-8500-1	8.95	4N33	3.95	ICM7045	24.95	LD110/111	25.00/set
AY-5-9100	17.50	8T20	7.50	ICM7207	7.50	95H90	11.95
AY-5-9200	14.95	8T97	2.00	ICM7208	22.00	MC3061P	3.50
AY-5-9500	4.95	HD0165	7.95	ICM7209	7.50	MC4016 (74416)	7.50
AY-5-2376	14.95	MCM6571	13.50	MK50240	17.50	MC1408L7	8.95
9374	1.95	MCM6574	13.50	DS0026CH	3.75	MC1408L8	9.95
82S115	25.00	MCM6575	13.50	TIL308	10.50		

CLOCK CHIPS

MM5309	$9.95
MM5311	4.95
MM5312	4.95
MM5314	4.95
MM5316	6.95
MM5318	9.95
MM5369	2.95
MM5841	9.95
CT7001	5.95

PARATRONICS

Featured on February's Front Cover of Popular Electronics

Logic Analyzer Kit Model 100A

$229.00/kit

Model 100A assembled $295.00

Model 100A — Model 10

- Analyzes any type of digital system
- Checks data rates in excess of 8 million words per second
- Trouble shoot TTL, CMOS, DTL, RTL, Schottky and MOS families
- Displays 16 logic states up to 8 digits wide
- See ones and zeros displayed on your CRT, octal or hexadecimal format
- Tests circuits under actual operating conditions
- Easy to assemble — comes with step-by-step construction manual which includes 80 pages on logic analyzer operation.

(Model 100A Manual - $4.95)

- Some applications are:
  - — Troubleshooting microprocessor address, instruction, and data flow
  - — Examine contents of ROMS
  - — Tracing operation of control logic
  - — Checking counter and shift register operation
  - — Monitoring I/O sequences
  - — Verifying proper system operations during testing

PARATRONICS TRIGGER EXPANDER - Model 10

Adds 16 additional bits. Provides digital delay and qualification of input clock and 24-bit trigger word. — Connects direct to Model 100A for integrated unit).

Model 10 Kit — $229.00
Model 10 Assembled — $295.00
Baseplate — $9.95
Model 10 Manual — $4.95

B+K PRECISION 3½-Digit Portable DMM



- Overload Protected
- .3" high LED Display
- Battery or AC operation
- Auto Zeroing
- 1mv, 1Va, 0.1 ohm resolution
- Overange reading
- 10 meg input impendence
- DC Accuracy 1% typical

Ranges: DC Voltage ±0-1000V/ AC Voltage: 0-1000V
Freq. Response: 50-400 HZ
DC/AC Current: 0-100mA
Resistance: 0-10 meg ohm
Size: 6.4" x 4.4" x 2"

Model 2800 $99.95

Comes with test leads, operating manual and spare fuse.

Accessories:

AC Adapter BC-28	$9.00
Rechargeable Batteries BP-26	20.00
Carrying Case LC-28	7.50

CSC 100 MHz 8-Digit Counter

- 20 Hz-100 MHz Range
- .6" LED Display
- Crystal-controlled timebase
- Fully Automatic
- Portable — completely self-contained
- Size — 1.75" x 7.38" x 5.63"
- Four power souces, i.e. batteries, 110 or 220V with charger 12V with auto lighter adapter and external 7.2-10V power supply

MAX-100 $134.95



ACCESSORIES FOR MAX 100:

Mobile Charger Eliminator use power from car battery — Model 100 — CLA $3.95

Charger/Eliminator use 110 V AC — Model 100 — CAI $9.95

CONTINENTAL SPECIALTIES

PROTO BOARD 6

$15.95

(6" long X 4" wide)



Other CS Proto Boards

PB100 - 4.5" x 6"	$ 19.95
PB101 - 5.8" x 4.5"	29.95
PB102 - 7" x 4.5"	39.95
PB103 - 9" x 6"	59.95
PB104 - 9.5" x 8"	79.95
PB203 - 9.75 x 6½ x 2¾	80.00
PB203A - 9.75 x 6½ x 2¾	129.95

(includes power supply)

PROTO CLIPS

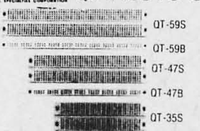
14 PIN	$4.50
16 PIN	4.75
24 PIN	8.50
40 PIN	13.75

DESIGN MATES

DM1 - Circuit Designer $69.95
DM2 - Function Generator $74.95
DM3 - RC Bridge $74.95

LOGIC MONITOR for DTL, HTL, TTL or CMOS Devices **$84.95**

CSC QT PROTO STRIPS



QT type	#holes	price
QT-59S	590	12.50
QT-59B	bus strip	2.50
QT-47S	470	10.00
QT-47B	bus strip	2.25
QT-35S	350	8.50
QT-35B	bus strip	2.00
QT-18S	180	4.75
QT-12S	120	3.75
QT-8S	80	3.25
QT-7S	70	3.00

Experimentor 300	$ 9.95
Experimentor 600	$10.95

$5.00 Minimum Order — U.S. Funds Only
California Residents — Add 6% Sales Tax

Spec Sheets - 25¢ — Send 35¢ Stamp for 1978 Catalog
Dealer Information Available

NOW OPEN SATURDAYS



1978 CATALOG NOW AVAILABLE

1021-A HOWARD AVE., SAN CARLOS, CA. 94070
PHONE ORDERS WELCOME — (415) 592-8097
All Advertised Prices Good Thru January

The Incredible "Pennywhistle 103"



$129.95 Kit Only

The Pennywhistle 103 is capable of recording data to and from audio tape without critical speed requirements for the recorder and it is able to communicate directly with another modem and terminal for telephone "hamming" and communications for the deaf. In addition, it is free of critical adjustments and is built with non-precision, readily available parts.

Data Transmission Method .....Frequency-Shift Keying, full-duplex (half-duplex selectable).
Maximum Data Rate ....300 Baud.
Data Format ....Asynchronous Serial (return to mark level required between each character).
Receive Channel Frequencies ...2025 Hz for space; 2225 Hz for mark.
Transmit Channel Frequencies ..Switch selectable: Low (normal) = 1070 space, 1270 mark; High = 025 space, 2225 mark.
Receive Sensitivity ....−46 dbm accoustically coupled.
Transmit Level ....−15 dbm nominal. Adjustable from −6 dbm to −20 dbm.
Receive Frequency Tolerance ...Frequency reference automatically adjusts to allow for operation between 1800 Hz and 2400 Hz.
Digital Data Interface ....EIA RS-232C or 20 mA current loop (receiver is optoisolated and non-polar).
Power Requirements ....120 VAC, single phase, 10 Watts.
Physical ....All components mount on a single 5" by 9" printed circuit board. All components included.

Requires a VOM, Audio Oscillator, Frequency Counter and/or Oscilloscope to align.

ERC AM/FM 8-Track Stereo Receiver With BSR Changer



- PLL System
- BSR Record Changer
- Slide Controls
- Automatic AFC Control
- 4 Speaker Output
- Walnut finish vinyl covered wood veneer with smoke dust cover

Size: 20"W x 9⅜"H x 15¼"D

Model 8365 $149.95

DIGITAL STOPWATCH

- Bright 6 Digit LED Display
- Times to 59 minutes 59.59 seconds
- Crystal Controlled Time Base
- Three Stopwatches in One Times Single Event — Split & Taylor
- Size 4.5" x 2.15" x .90" (4½ ounces)
- Uses 3 Penlite Cells



Kit — $39.95
Assembled — $49.95
Heavy Duty Carry Case $5.95

Stop Watch Chip Only (7205) $19.95

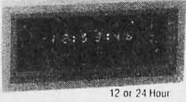
IMC 3½ DIGIT DPM KIT



- New Bipolar Unit
- Auto Zeroing
- .5" LED
- Auto Polarity
- Low Power
- Single IC Unit

Model KB500 DPM Kit $49.00
Model 311D-5C-5V Power Kit $17.50

JE700 CLOCK

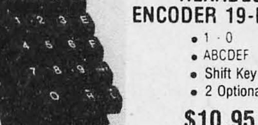


12 or 24 Hour

The JE700 is a low cost digital clock, but is a very high quality unit. The unit features a simulated walnut case with dimensions of 6" x 2½" x 1". It utilizes a MAN72 high brightness readout, and the MM5314 clock chip.

115 VAC *KIT ONLY* **$16.95**

HEXADECIMAL ENCODER 19-KEY PAD

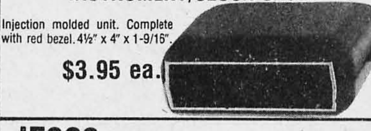
- 1 - 0
- ABCDEF
- Shift Key
- 2 Optional Keys

$10.95 each

INSTRUMENT/CLOCK CASE

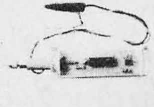
Injection molded unit. Complete with red bezel. 4½" x 4" x 1-9/16".

$3.95 ea.



JE803 PROBE

The Logic Probe is a unit which is for the most part indespensible in trouble shooting logic families TTL, DTL, RTL, CMOS. It derives the power it needs to operate directly off of the circuit under test, drawing a scant 10 mA max. It uses a MAN3 readout to indicate any of the following states by these symbols (H) - 1 (LOW) - o (PULSE) - P. The Probe can detect high frequency pulses to 45 MHz. It can't be used at MOS levels or circuit damage will result.

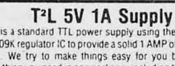


$9.95 Per Kit

printed circuit board

T^2L 5V 1A Supply

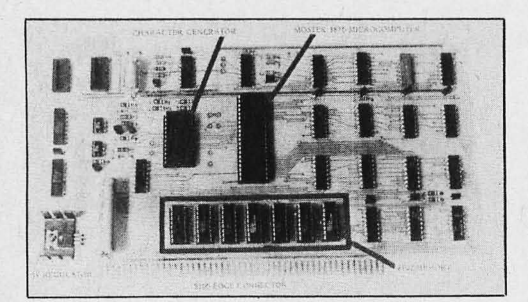




This is a standard TTL power supply using the well known LM309K regulator IC to provide a solid 1 AMP of current at 5 volts. We try to make things easy for you by providing everything you need in one package, including the hardware for only **$9.95 Per Kit**

Circle 55 on inquiry card.

Video Board Features Dedicated Microcomputer



This new video interface board, designed around the Mostek 3870 chip, illustrates how a dedicated microcomputer can be used to reduce costs and implement additional features not easily realized with conventional logic. Operating under the control of the program in its built-in memory, the 3870 helps provide ASCII and Baudot serial interfaces, multiple data rates up to 300 bps, full XY cursor control, screen clear, clear to end of line, page mode and autoscroll. Though the same size as an Altair (S-100) bus, the board uses only the power connections, and includes a rectifier and filter for stand alone use with a 6.3 VAC, 1 A transformer. Designated the SCT-100, the board is available from Vectron, POB 20887, Dallas TX 75220, (214) 350-5291, in three forms: an assembled and tested unit for $185, a complete kit for $155, and a printed circuit board, 3870, and character generator ROM for $85.■

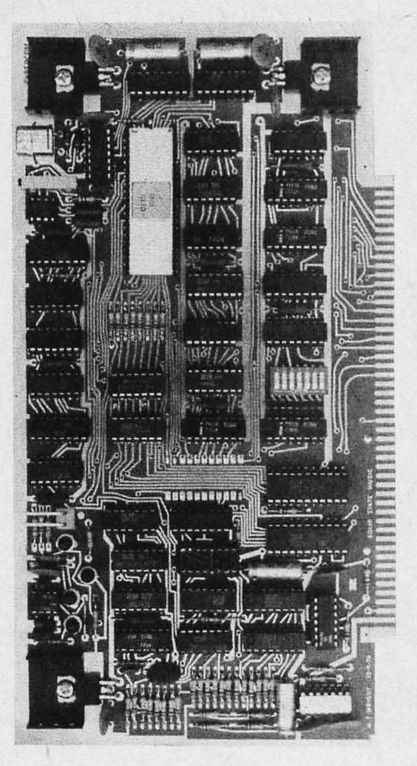
Circle 551 on inquiry card.

A Synthesizer and Music Language

The Solid State Music Synthesizer Board (SB-1) is a waveform synthesizer card designed to interface with the S-100 bus. With this card, a microcomputer may be programmed to play a monophonic solo in an instrumental "voice" that is controlled by software. Polyphonic capability is provided for in the MUX language for multiple cards. The music is written by the user by means of high level language interpreter called MUX which is entered into the system via an ASCII keyboard, paper tape, floppy or other input medium.

The MUX language contains the operational routines and lookup tables to generate the following:

a. the musical note
b. the voicing envelope (attack and decay)
c. loudness or volume commands
d. octave selection (9 octave range)
e. memory retention of two waveforms
f. waveforms selection (voicing change) 8 in memory
g. repetition effects
h. 1/64th note through whole note
i. dotted note, double dotted note
j. time signature
k. repeat measure
l. key signature



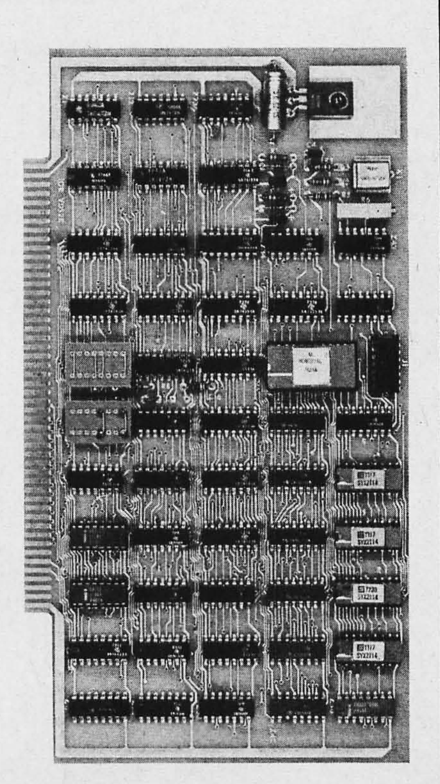
Any 256 byte increment from 8000 hexadecimal to FF00 hexadecimal can be used for this board by presetting a switch on the card. The kit costs $250, and an assembled and tested version is $350. Contact Solid State Music at 2102A Walsh Av, Santa Clara CA 95050, (408) 246-2707.■

Circle 552 on inquiry card.

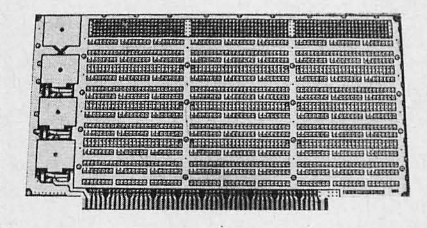
Video Output for Scope or Monitor

The VDS2K video interface board includes all address decoding necessary for direct display of characters from memory, or for display of characters received one at a time from an IO port, with automatic cursor updating. Video output can be either in the form of a composite video signal, appropriate for a video monitor, or a set of "XYZ" TTL level signals appropriate for the horizontal, vertical and intensity inputs of many oscilloscopes. This Altair (S-100) bus interface displays 30 lines of 64 characters, and also has a 128 byte nondisplayable buffer memory. Upper case, lower case and Greek characters are provided in a 7 by 9 dot matrix. The VDS2K kit is $399 from IOR, Box 28823, Dallas TX 75228, (214) 358-2671.■

Circle 553 on inquiry card.



Wire Wrappable Prototyping Board



This Altair (S-100) bus prototyping board features an all wire wrappable format, a dedicated regulator and three additional etched TO-220 locations, prenumbered integrated circuit locations, and provisions for filter capacitors and flat cable connectors for interfacing purposes. The board will accommodate all sizes of integrated circuits, from as many as 81 14 or 16 pin sockets to as many as 12 36 or 40 pin sockets. An instruction manual is included. The board is $39.95 from Orange Digital Electronics, POB 2311, Mission Viejo CA 92675.■

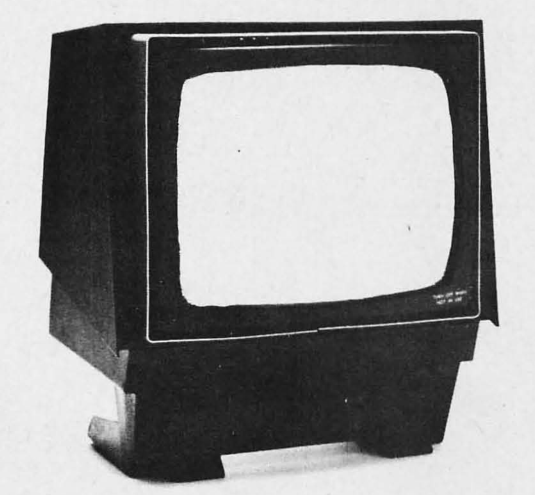
Circle 554 on inquiry card.

Fantastic $avings on Terminal Components

We have obtained a fairly large supply of professional CRT video monitors, encased in attractive metal cabinets with a simulated mahogany finish. We do not know the bandwidth capabilities of these 12" (diagonal) units; we have used them, however, to test our 24 x 80 video display board and have found them perfectly satisfactory. These units were manufactured by or for one of the largest data communications firms in the country. We are not allowed to use the name, and the nameplates had to be removed. Many of you have probably seen these units functioning. They are equipped with a standard video connector and have all the normal controls. They operate at 110 V, 60 cycles.

The units are in reasonably good condition cosmetically, although nearly all of them have a defect in the plastic anti-glare screen in front of the CRT tube. This screen could be readily removed or replaced.

We estimate that these units would sell new for between $150 and $200. We are offering them for sale in both functional and in non-functional condition.



12CRT Used, operable* .... **$ 59.95**

12CRTNF Used, complete, known non-functioning ..... **$ 39.95**

*Units have been tested but are sold as-is. They are not represented as reconditioned units and may require minor repairs or adjustments.

Add the following charges for handling-shipping-insurance:
$2.50 Eastern Time Zone $3 Central $4 Mountain $5 Pacific

MiniMicroMart, Inc. also stocks a complete line of kits for building video display units.
Write for information



COMMERCIAL MODEMS — *Limited Supply* — Acoustical coupler type and direct hard wire variety. Both operate at standard Bell Telephone frequencies, at up to 300 baud; they are Bell 103 compatible. They appear to be in new or equal-to-new condition. They are intended for communicating from a terminal to a time-share computer. Standard RS232C type connectors are supplied.

MDACP (acoustical)	$ 59.95
MDHW (hard wire)	44.95
MDACP-NF (used, suspect non-functional)	39.95
MDHW-NF (used, suspect non-functional	24.95

Add $2 for handling-shipping-insurance.

KEYBOARDS— *Limited Supply*
Attractive communications style keyboards;, some in cases which match the monitor shown above. They are not ASCII encoded but the coding could be changed in software with PROMs or by replacing the circuitry with an encoding I.C. They key switch modules are of Cherry manufacture with an excellent feel. A schematic and limited modification information is supplied.



KBN brand new, in case	$ 37.95
KBU used, in case	27.95
KBUD used, in case, minor cosmetic defects	22.95
KBUNC used, no case	19.95

Add $2.50 for handling-shipping-insurance.

Write for free 64-page catalog featuring hundreds of items for minicomputer systems.

MiniMicroMart, Inc. 1618 James Street, Syracuse, N.Y. 13203 (315) 422-4467

Circle 67 on inquiry card.

What's New?

MASS STORAGE

New Drive for Miniature Data Cartridges

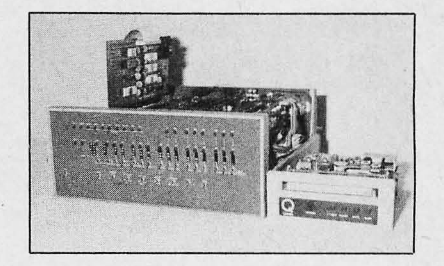


Utilizing the 3M DC100A miniature data cartridge, this new tape transport measures only 3 by 4 by 4.125 inches (7.6 by 10.2 by 10.5 cm) and costs as little as $250 in single quantities, including "intimate" electronics. The Model 200 Minidrive can record up to 772,000 bytes of data on a single cartridge, at a recording density of 1600 bits per inch and a data rate of 48,000 bits per second. The "intimate" electronics include the motor drive and read head amplifiers, the write head driver, optical tachometer for tape speed control, track selection logic, solid state beginning and end of tape detectors, and file protect and cartridge in place detectors. A servo and data card, peripheral interface adapter card, control logic card, and card cage with printed circuit backplane can be added to form a complete controller and interface. The manufacturer supplies direct interfacing for the Intel 8080 and Motorola 6800 microprocessors, as well as interfaces tailored to the LSI-11, Nova, Interdata and Altair computers. One controller can "daisy chain" up to four Minidrives, providing access to as much as 1.3 million bytes of storage with an average access time of 9 seconds.

In single quantities, the 1 track low density (168,000 byte capacity) version of the Model 200 sells for $250, while the 2 track high density (772,000 byte capacity) version is priced at $350. A complete 1 track drive and controller costs about $485 in single quantities. Substantial quantity discounts are available to OEM buyers. The Model 200 is made by the Quantex division of North Atlantic Industries Inc, 200 Terminal Dr, Plainview NY 11803, (516) 681-8350.■

Circle 564 on inquiry card.

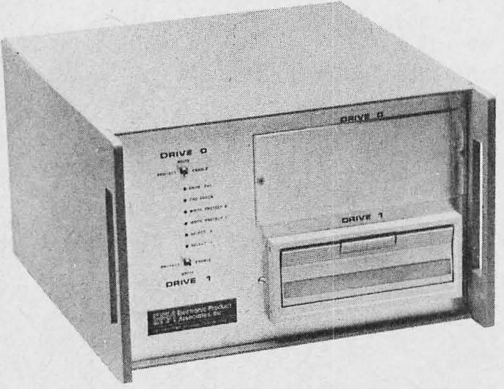
3M Cartridge Drive Interface



This Altair (S-100) bus compatible interface board controls up to eight Quantex Model 600 3M cartridge tape drives. The board includes software in ROM to dump and load named files from anywhere in memory, search for a file name or list all files on a cartridge, rewind, unload, erase, skip blocks, and other functions. Data is recorded with phase encoding using a cyclic redundancy character check for error detection and correction. The Quantex Model 600 drive uses the DC-300A tape cartridge, containing 300 feet of ¼ inch tape. Data is recorded at 48,000 bits per second, 1600 bits per inch serially on 1, 2 or 4 tracks. With proper formatting more than 2 million bytes can be stored on a cartridge. The AQ-86 interface board is priced at $425, and a single Quantex Model 600 cartridge drive at $825, from Galt Electronics, 9924 Lanham Severn Rd, Seabrook MD 20801, (301) 459-1496.■

Circle 568 on inquiry card.

Floppy Controller Includes Status Panel



The EPA Micro-68b floppy disk system now includes a disk status monitoring panel and write protect switches. Available in either single ($2495) or dual ($3295) configurations, the Micro-68b disk includes the interface necessary to plug into either the 6800 exorciser or the Altair (S-100) bus. The status panel contains indicators for drive selection, write protection, CRC error and disk status. Housed in a ruggedized, light blue aluminum cabinet to match the Micro-68b computer, the unit is available from Electronic Product Associates Inc, 1157 Vega St, San Diego CA 92110, (714) 276-8911.■

Circle 567 on inquiry card.

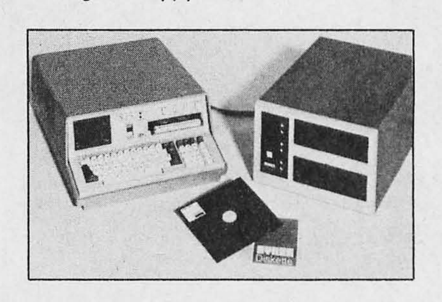
At Last, a Solid State Disk



40 times faster than the fastest electromechanical rotating disk memory, the CCDISC contains a solid state charge coupled device memory with a capacity of up to 1 million bytes in 128 K byte increments. Capacities up to four megabytes can be achieved by daisy chaining these solid state "disks." Average access time is 250 μs, making the CCDISC ideal for paging, program swapping, timesharing and distributed network applications. The unit is plug compatible with the rotating magnetic head-per-track disk memory interfaces made by the manufacturer, Alpha Data Inc, 20750 Marilla St, Chatsworth CA 91311, (213) 882-6500. CCDISC memories are available eight weeks after receipt of order and cost $3195 in OEM quantities.■

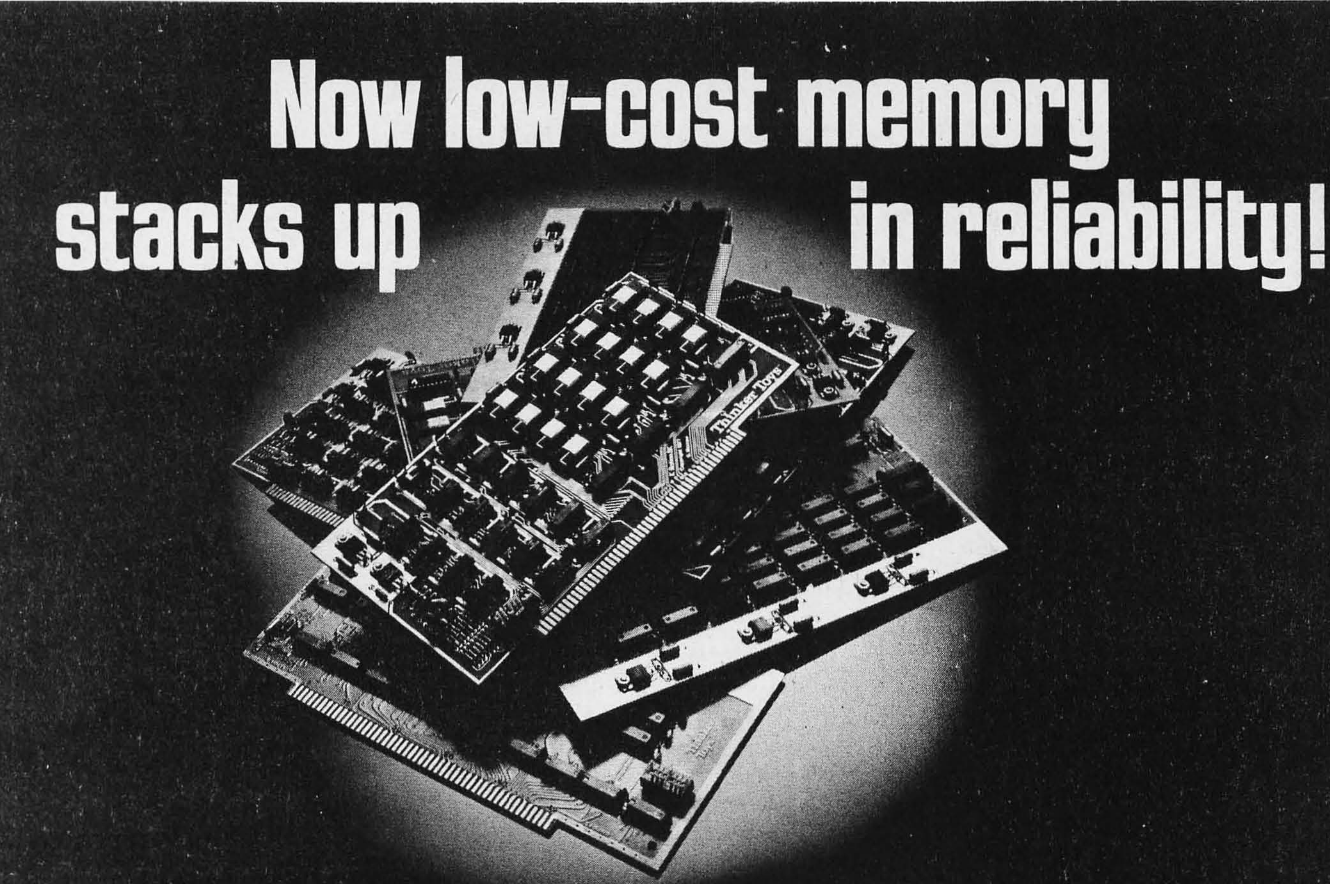
Circle 566 on inquiry card.

Attention IBM 5100 Users: An Intelligent Floppy Disk



This floppy disk storage system includes its own microprocessor and plugs directly into the IBM 5100 serial IO port, requiring no changes to the 5100 hardware or software. The CommStor/5100 has its own file management system controlled by simple commands and is compatible with both BASIC and APL (files created under BASIC can be read under APL and vice versa). The floppy disk format is compatible with the IBM 3740. The system comes with a 5100 tape cartridge containing ten BASIC key files and 14 APL functions. A single drive system is priced under $3000, and a dual drive system under $4000, from Sykes Datatronics Inc, 375 Orchard St, Rochester NY 14606, (716) 458-8000.■

Circle 569 on inquiry card.



Now low-cost memory stacks up in reliability!

Introducing a new generation of ECONORAM* dynamics with SynchroFresh™ reliability

Meet ECONORAM* III with SynchroFresh™, the 8Kx8 dynamic memory for S-100 bus computers that really works. And uses less than half the power of static designs. And costs just $149 for an assembled 8K.

Unlike previous attempts at building a low-cost dynamic memory, ECONORAM* III is entirely reliable ... because of SynchroFresh™, a new approach to memory refresh that is simple, elegant and totally effective.

SynchroFresh™ was invented by George Morrow, designer of the original ECONORAM*. Instead of arbitrarily interrupting your CPU to perform memory refresh cycles, Morrow designed SynchroFresh™ to weave refresh invisibly into the natural timing of the S-100 bus. SynchroFresh™ circuitry simply monitors your computer's machine states, utilizing all of the normal opportunities for memory refresh. It's that simple.

And simplicity means reliability and dramatically lower cost. That's why a SynchroFresh™ design was chosen for the first ECONORAM* dynamic, to follow in the footsteps of the largest-selling static memories for personal computers.

ECONORAM* III with SynchroFresh™ is an 8Kx8 dynamic board, configured as two individually addressable 4K blocks for flexibility. It is available assembled, tested and warranteed for one full year for just $149. This unprecedented warrantee offers a full refund of purchase price if ECONORAM* III does not run reliably with your S-100 CPU—evidence of our confidence in its performance.

It is also available as a kit with complete assembly instructions and documentation for $159.

ECONORAM* III with SynchroFresh™, in assembled or kit form, may be ordered directly from Thinker-Toys™. Write 1201 10th Street, Berkeley CA 94710 or call (415) 527-7548. Call BAC/MC orders toll-free to 800-648-5311. Or ask your computer store to order it for you.

NEW LOW PRICE

$149

8K assembled, tested, warranteed 1 year

A product of Morrow's Micro-Stuff for

Thinker Toys™

*ECONORAM is a trademark of Godbout Electronics.

Circle 68 on inquiry card.

Classified Ads

FOR SALE: Dura 941 data terminal, includes IBM Selectric typewriter with BCD coding, paper tape punch and reader. Unit is in good working order except for punch which has an electrical problem. For sale as is at $300, prints and instructions included. Freight collect. Will make an ideal hard copy printer even without the punch, and where else can you get a Selectric typewriter for $300? Write Jim Parsly, Apt 305, 401 W Johnson St, Philadelphia PA 19144.

FOR SALE: completely assembled and tested Solid State Music 16 K true static memory board; fast, 200 ns; low power, .55 A @ + 8 V; fully buffered with memory protect in 4 K blocks and automatic unprotect on power up. $500 or best offer. Tim Wedlake, POB 3074, San Leandro CA 94578.

FOR SALE: One MITS serial IO board, Morrow's cassette interface board with all options. Will accept best offer for each or both. Victor Chinn, 1618 Milvia, Berkeley CA 94709.

WILL TRADE: A working SC/MP (kit built) and working keyboard as sold by NS for $200 for a good frequency counter. Also for sale: A 8223 PROM programmer, complete except for 12 VDC, 300 mA furnished by user, price: $20. James Upchurch, 3407 Dauphine Dr, Sebring FL 33870.

WANTED: Qume or Diablo IO printer to run with a Cromemco Z-80 system. Also, does anyone have any information on how to interface an old Friden Flexowriter SPD to a microsystem? William Brady, 156 Drakes Ln, Summertown TN 38483.

FOR SALE: Altair 680B assembled and tested, also high speed paper tape reader and high speed paper tape punch. The whole works for $450. Dave Woodhouse, 172 Hickory Creek Dr, Frankfort IL 60423. After 7 PM call (815) 469-9316.

FOR SALE: IMSAI 8080 microcomputer, 22 slot mother board, 8 K programmable memory, MIO board (serial, parallel and cassette interface board), professionally assembled and tested in excellent condition. Complete with input and output cables and all manuals. Call (215) 643-2467 after 5 PM. William Schmidt, 1426 Jonathan Way, Ambler PA 19002.

FOR SALE: OSI 400 System with: 400 CPU board, 440 video graphics board, 430 cassette IO board, 11 K RAM, keyboard, power supply, cases, and extras. Fully socketed. $750 or offer. B Fabry, Rt 2, Box 22A, Morgantown WV 26505. (304) 296-2485.

Readers who have equipment, software or other items to buy, sell or swap should send in a clearly typed notice to that effect. To be considered for publication, an advertisement should be clearly noncommercial, typed double spaced on plain white paper, and include complete name and address information. These notices are free of charge and will be printed one time only on a space available basis. Insertions should be limited to 100 words or less. Notices can be accepted from individuals or bona fide computer users clubs only. We can engage in no correspondence on these and your confirmation of placement is appearance in an issue of BYTE.

Please note that it may take three or four months for an ad to appear in the magazine.■

FOR SALE: Unfinished computer project worth much more than $800 of RM 8080, 4 K programmable memory, TV terminal, Philips cassette 60 tape deck, edge connectors, TTL, CMOS and Intel ICs, designing and specification books, capacitors, keyboard, more. Goes for $550 or best offer. T P Douglas, POB 1012-V, La Junta CO 81050. (303) 384-9594.

BACK ISSUES WANTED: BYTE numbers 7 thru 10 (March thru June 1976). Prefer undamaged originals, but will accept Xerox or microfiche copies with publisher's permission. Send your asking price and description to Carl S Zimmerman, POB 53, APO NY 09378.

FOR SALE: National's Novus 4520 Scientist: RPN 4 level stack, power and root functions, all trig functions, all log functions, etc, Operations Guide, AC charger, carrying case, $20. Edwin A Zaratkiewicz, 3708 Hampton Way, Kent WA 98031.

JOB WANTED: I am looking for interesting and challenging work in the computer field. I have worked with computers for over six years, know most common assembler and compiler languages, and will be graduating from the University of Pennsylvania in May with a degree in computer engineering. If you are trying to find a person to handle a tough but interesting job, please write to me for my complete resume. Steve Masticola, POB 951, 3901 Locust Walk, Philadelphia PA 19174. All offers carefully considered.

FOR SALE: Miniterm MERLIN graphics display board, S-100, new, assembled, $269. Mark Dahmke, 1393 8th St, David City NB 68632. (402) 367-4367 after 6 PM.

FOR SALE: 6800 system with processor board, 20 K programmable memory, video interface, and four serial ACIA ports for KC standard, RS232, TTY. One 8 bit parallel port. 1.25 K EPROM with debugger, assembler, editor, load and dump. Manuals, schematics, software. Factory assembled. $1250. David Demorest, 12697 Graton Rd, Sebastopol CA 95472. (707) 823-1698.

FOR SALE: Digital Equipment Corporation DK8EP programmable real time clocks $395. Other PDP8e modules for sale or trade. Free list. Want 8 K core or any other DEC peripherals or components. K2DCY. 11 Squire Hill Rd, North Caldwell NJ 07006.

FOR SALE: Altair 8800a, 8 K dynamic memory, cassette interface card, all mother boards, edge connectors, and card guides. Unit is completely functional, all cards are standard MITS items. A bargain at $750. Bill Shappley, 6395 Forest Grv, Memphis TN 38138. (901) 682-1897 after 7 PM.

FOR SALE: Issues 1, 2, 3 and 4 of BYTE, perfect condition, to the highest bidder. Also June 1976 to May 1977 inclusive of BYTE. Specify your bid and the issues you desire. Doug Dierdorf, 103 N Park Dr, Wilmington DE 19809.

WANTED: An inexpensive secondhand DecWriter II for use on a time sharing system. Any condition except broken is acceptable. I'm willing to pay up to $1,100. Send all offers to Scott Johnson, 18 Coraway Rd, Setauket NY 11733.

TTY DONATION? Elementary school needs remote terminal for kindergarten through sixth grade computer math course. Any donation in working (or fixable) shape will be appreciated by Maria Hastings Public School, Lexington MA 02173. Call collect to Richard E Zapolin, (617) 271-2534.

FOR SALE: Altair 8800 with one 4 K static ram implemented, and one 1 K static ram board loose, $400; I pay postage. James Jones, 220 N Blvd #17, Gunnison CO 81230.

FOR SALE: BYTE Issues 2 thru 9 (October 75 thru May 76), fine condition. Best offer. Mel Raab, Rm 4731 Boelter Hall, UCLA, Los Angeles CA 90024.

FOR SALE: Godbout 8 K EconoROM, populated with 4 K of 5204 PROMS now containing Editor/Assembler/Monitor, a steal at $200 (current cost $265). OAE paper tape reader fully assembled and operational, $60. Call Mitchell (after 3:00 PM, weekdays) at (617) 963-5578.

FOR SALE: ASCIISCOPE 12 by 80 CRT with built in acoustic coupler $550 with documentation, S S Music MB3 with 4 K 1702A $115, MITS 4 K dynamic $100, Processor Technology VDM $155, 3 P+S $115, OAE Tape Reader $60, IMSAI 4 K Static $100. All assembled fully socketed and factory checked out. K R Roberts, 10560 Main St, Suite 515, Fairfax VA 22030.

FOR SALE: Cromemco Cyclops TV camera with sophisticated controller interface to S-100 bus, assembled $300, save 50%. G Lyons, 280 Henderson, Jersey City NJ 07302. (201) 451-2905.

FOR SALE: Five 4 K S-100 static memory boards. Factory assembled and still on warranty, one never out of box. I am switching to 16 K boards. $100 each. No personal checks or cash please. Al Marshall, 408 Oakwood, Angola IN 46703.

SELL OR SWAP: I'm cleaning out Teletype Models 33 and 38, converted Selectric IO typewriter, Telewriter portable terminal (SCM electric portable adapted as RS232 IO), all in top condition, also 10 years of *QST* and *American Journal of Physics* (teacher's) magazines, foreign language learning tapes, telephone and radio equipment. Send SASE for list with pictures and specifications. M Boltzman, POB 2525, Plainfield NJ 07060.

FOR SALE: Make offer for complete set of BYTEs, September 1975 thru July 1977, all issues in like new condition; package deal only. C Reece, 4924 Brandenburg, POB 80712, Lewisville TX 75056. (214) 370-0973.

FOR SALE: Altair 8800A with IMSAI 28 A power supply installed in original cabinet. Comes with serial IO board, four 4 slot expander boards, 12 edge connectors, fan, 4 K and 8 K BASIC, assembly language package, and many games. With 12 K memory, $1100 or 32 K memory and Tarbell cassette interface, $2000. Everything carefully assembled and working perfectly. Michael Favitta, 4 Sherwood Forest Rd, Albany NY 12203. (518) 456-8717.

4 K MEMORY BOARDS: Solid State Music (MB-2) assembled, socketed, tested, with full speed 2102s. Two available. $75 each. TTY paper tape. 1 inch wide, 8 inch diameter roll, lightly oiled buff. Perfect for ASR-33. $10 per 28 roll case + UPS on 48 lbs, Dan S Parker, 1007 3rd St #3, Davis CA 95616. (916) 758-2341 after 6:00 PM. Orders shipped within 24 hours.

FOR SALE: Data modems. One new, acoustically coupled, never used, cost $270. Sacrifice at $195. One used, tested, and in perfect working order. $75. Call evenings. C Lopez (714) 272-4381.

WANTED: First seven BYTEs. Will consider additional issues in order to get first seven. Good copies acceptable also. Send quotes to: Joseph Heck, 101 Wachusetts St, Jamaica Plain MA 02130.

FOR SALE: Texas Instruments Silent 700 Terminal, Model KSR733 with modem cable, maintenance manual (worth $25) and four rolls of paper. Original price $2000. Will sell for $900 or best offer. Terry Higbee, 5071 Scott Cir, LaPalma CA 90623. (714) 523-2548.

FOR SALE: HP 9830A programmable calculator with memory option 275, 9866A line printer, Data Comm interface, and the following ROMs: String Variables, Advanced Prog II, Data Comm I and Data Comm III. Perry B Fink, 82 S Deere Park Dr, Highland Park IL 60035. (312) 432-2998.



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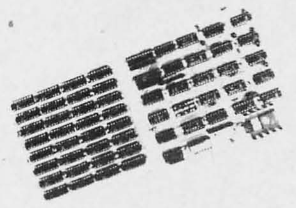
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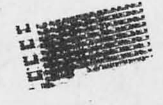
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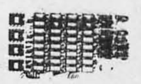
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AC XFMR — **$1.50 Case $3.50**

5 Digit Countdown Utility Darkroom Timer Kit

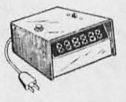
Features: Large LED 1/2" displays oper. from 0.1 sec. to 59 min. 59.99 sec. 5A-115V. Relay included to control appliances. Operates on 115V AC. Displays can be turned off for total darkness while counting. All necessary parts included.
Special design case $3.75.



$44.95

6 Digit General Purpose or Computer Timer Kit — $29.95

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BOMB—BYTE's Ongoing Monitor Box

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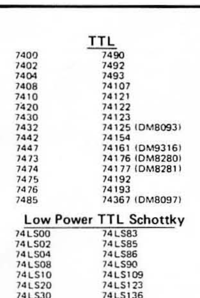
BOMB Analysis for the October 1977 Issue

First place (and a $100 bonus) went to David A Higgins' article on "Structured Program Design" using Warnier-Orr diagrams, page 146. His article had a rank of 1.37 standard deviations above the mean of 13 articles. Second place and a $50 bonus went to David Kruglinski's "How to Implement Space War," page 86. His article ranked 1.26 standard deviations above the mean. The standard deviation in October's analysis was 24% of the mean, indicating a relatively wide spread of evaluations. Be sure to indicate your reactions to this month's issue by rating each article on the BOMB evaluation card and forwarding it to our office. The BOMB card is your direct line to the editors' desks.■



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7408	74107
7410	74121
7420	74122
7430	74123
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7442	74154
7447	74161 (DM9316)
7473	74176 (DM8280)
7474	74177 (DM8281)
7475	74192
7476	74193
7485	74367 (DM8097)

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74LS02	74LS85
74LS04	74LS86
74LS08	74LS90
74LS10	74LS109
74LS20	74LS123
74LS30	74LS136
74LS32	74LS138
74LS73	74LS151
74LS74	74LS175
74LS75	74LS367

C/MOS

4000	4029
4001	4044
4010	4046
4011	4049
4013	4050
4016	4051
4017	4069
4020	4071
4023	4081
4024	4511

LINEAR

LM301V	LM340T-15(7815)
LM307V	LM555V
LM309K	LM556N
LM311V	LM567V
LM320K-5(7905)	LM723N
LM320T-5(7905)	LM739N
LM320T-12(7912)	LM741V
LM320T-15(7915)	LM747N
LM339N	LM1458V(5558V)
LM340T-5(7805)	LM1556V
LM340T-12(7812)	LM3900N(CA3401)

MICROPROCESSOR

Z-80	2101
8080A	2102
8212	21L02
8224	7489
8228	MM5262
6800	1702A
6810	82S23
6830	2708
AY-5-1013	DM8835N
2513/2140	N8T97

DIODES

IN751	IN4148(IN914)
IN4733	IN4001
IN4734	IN4004
IN4742	IN4007
IN4744	MDA-980-3

TRANSISTORS

C106B1	2N3055
2N2222A	2N3904
2N2907A	2N3906
MJE2955	2N5129
MJE3055	2N5139

RESISTORS

ASST 1	ASST 5
ASST 2	ASST 6
ASST 3	ASST 7
ASST 4	

CAPACITORS

Aluminum Electrolytic

1mfd 50V	100mfd 50V
4.7mfd 50V	220mfd 50V
10mfd 50V	470mfd 50V
22mfd 50V	1000mfd 25V
47mfd 50V	2200mfd 16V

Ceramic Disc

10pf 50V	.001mfd 50V
47pf 50V	.0047mfd 50V
100pf 50V	.01mfd 50V
220pf 50V	.022mfd 50V
330pf 50V	.047mfd 50V
470pf 50V	.1mfd 50V

Dipped Tantalum

.1mfd 35V	2.2mfd 25V
.22mfd 35V	3.3mfd 25V
.33mfd 35V	4.7mfd 25V
.47mfd 35V	6.8mfd 25V
.68mfd 35V	10mfd 25V
1mfd 35V	15mfd 25V
1.5mfd 35V	33mfd 25V

SWITCHES

SPST 4 sta. dip	SPDT push button
SPST 8 sta. dip	SPDT push button
SPDT on-off-on toggle	SPST push button
	SPST push button
SPDT on-none-on toggle	SPST push button
	DPDT slide
DPDT on-off-on toggle	DPDT on-none-on toggle

SOCKETS

8 pin low profile	14 pin wire wrap
14 pin low profile	16 pin wire wrap
16 pin low profile	24 pin wire wrap
24 pin low profile	40 pin wire wrap
40 pin low profile	TO-3 Socket
Molex Pins	TO-5 Socket

LEDS

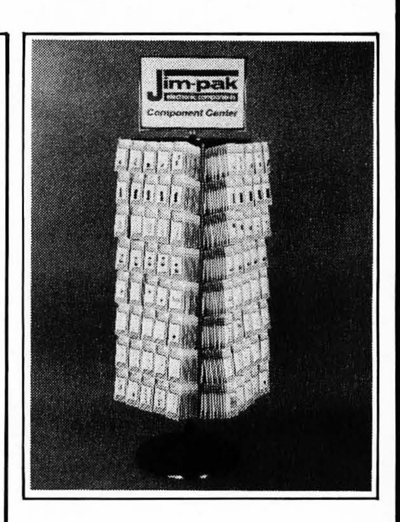
Display	Discrete
5x7 dot matrix	.600 com. anode
.300 com. anode	.600 com. cathode
.300 com. cathode	.200 LED Lamp-red

CONNECTORS

DB 25P Plug	DB25S Socket

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CMOS/Linear Data Book
Microprocessor/LED Data Book
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San Jose — *Sunnyvale Electronics*
Vallejo — *Zackit*
Walnut Creek — *Byte Shop Computer Store*
CANADA
Alberta (Calgary) — *The Computer Shop*
CONNECTICUT
Bridgeport — *Computer World*
FLORIDA
Orlando — *Altair Computer Center of Orlando*
Tampa — *AMF Electronics*
Tampa — *Microcomputer Systems*
FRANCE
Paris — *Computer Boutique*
GEORGIA
Atlanta — *Atlanta Computer Mart*
HAWAII
Aiea — *Delcoms Hawaii*
Honolulu — *Integrated Circuit Supply*
IDAHO
Idaho Falls — *Audiotronics*
ILLINOIS
Evanston — *Itty Bitty Machine Co.*
Groveland — *Moyer Electronics*
Mount Prospect — *Tri-State Electronics*
Oak Park — *Spectronics Inc.*
INDIANA
East Chicago — *Acro Electronics*
Hammond — *Quantum Computer Works*
LOUISIANA
Baton Rouge — *Davis Electronics Supply*
MARYLAND
Baltimore — *Computer Workshop of Baltimore*
Baltimore — *Everything Electronics*
Rockville — *Computer Workshop*
Towson — *Computers, Etc.*
MASSACHUSETTS
Medford — *Tufts Electronics*
North Adams — *Electronics Service Center*
Waltham — *Computer Mart Inc.*
MICHIGAN
Lansing — *Fulton Radio Supply*
MINNESOTA
Duluth — *Northwest Radio of Duluth*
Eagan — *Dacom Amateur Radio Center*
MISSOURI
Parkville — *Computer Workshop of Kansas City*
MONTANA
Billings — *Conley Radio Supply*
NEBRASKA
Lincoln — *Altair Computer Center*
Omaha — *Omaha Computer Store*
NEVADA
Las Vegas — *Century 23*
NEW JERSEY
Hoboken — *Hoboken Computer Works*
Ramsey — *Typetronic Computer Store*
NEW YORK
Albany — *Fort Orange Electronics*
New York — *The Computer Stores Inc.*
New York — *Computer Mart of New York*
Troy — *Trojan Electronics*
White Plains — *The Computer Corner*
NORTH CAROLINA
Raleigh — *Byte Shop of Raleigh*
OHIO
Bucyrus — *Mead Electronics*
Cincinnati — *Digital Design*
Steubenville — *Hosfelt Electronics*
OKLAHOMA
Guymon — *Sound Service*
Oklahoma City — *Bits, Bytes & Micros*
OREGON
Beaverton — *Altair Computer Center*
Coos Bay — *Herrick Electronix*
Ontario — *Miller Electronics*
PENNSYLVANIA
Hershey — *Microcomputer Systems Inc.*
Murraysville — *Computer Workshop of Pittsburgh*
RHODE ISLAND
Cranston — *Jabbour Electronics City*
Pawtucket — *Jabbour Electronics City*
SOUTH CAROLINA
No. Charleston — *Technical Services Inc.*
TENNESSEE
Memphis — *Sere-Rose & Spencer Electronics*
Oak Ridge — *Computer Denn*
TEXAS
Dallas — *Computer Shops Inc.*
Houston — *Altair Computer Center*
Houston — *Interactive Computers*
San Antonio — *Sherman Electronics Supply*
VIRGINIA
Alexandria — *Computer Hardware Store*
Alexandria — *Computers Plus*
Richmond — *Computers-To-Go*
Springfield — *Computer Workshop of North Virginia*
WASHINGTON
Bellevue — *Altair Computer Center*
Longview — *Progress Electronics*
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Spokane — *Personal Computers*
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Morgantown — *Electro Distributing Co.*

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